ACADEMIC REGULATIONS (R-25)
COURSE STRUCTURE
AND
DETAILED SYLLABI

M. Tech Regular (Full-Time) Two Year Post Graduate Degree Programme

(For the Batches Admitted from the Academic year 2025-2026)

VLSI DESIGN

ELECTRONICS AND COMMUNICATION ENGINEERING

SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY (AUTONOMOUS)

Accredited by NBA, New Delhi & NAAC A^{+}, Bengaluru │Affiliated to JNTUA, Ananthapuramu,

Recognized by the UGC under Section 12(B) and 12(F)│ Approved by AICTE, New Delhi.

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FOREWORD

The autonomy conferred Sri Venkateswara College Engineering and technology by JNT University, Ananthapuramu based on performance as well as future commitment and competency to impart quality education. It is a mark of its ability to function independently in accordance with the set norms the monitoring bodies UGC and AICTE. It reflects the confidence of the affiliating University in the autonomous institution to uphold and maintain standards it expects to deliver on its own behalf and thus awards degrees on behalf of college. Thus, an autonomous institution is given the freedom to have its own curriculum, examination system and monitoring mechanism, independent of the affiliating University but under its observance.

Sri Venkateswara College of Engineering and Technology is proud to win the confidence of all the above bodies monitoring the quality in education and has gladly accepted the responsibility of sustaining, the standards and ethics it has been striving for more than a decade in reaching its present standing in the arena of contemporary technical education. As a follow up, statutory bodies like Academic Council and Boards of Studies are constituted with the guidance of the Governing Body of the College and recommendations of the JNTUA, Ananthapuramu to frame the regulations, course structure and syllabi under autonomous status.

The autonomous regulations, course structure and syllabi have been prepared after prolonged and detailed interaction with several expertise solicited from academics, industry and research, to produce quality engineering graduates to the society.

All the faculty, parents and students are requested to go through all the rules and regulations carefully. Any clarifications needed are to be sought at appropriate time and with principal of the college, without presumptions, to avoid unwanted subsequent inconveniences and embarrassments. The cooperation of all the stake holders is sought for the successful implementation of the autonomous system in the larger interests of the college and brighter prospects of engineering graduates.

Principal

INSTITUTE VISION

To carve the youth as dynamic, competent, valued and knowledgeable professionals who shall lead the Nation to a better future and to mould the institution into a Center of Academic Excellence and advanced Research.

INSTITUTE MISSION

- To provide quality education, student-centered teaching-learning processes and state-of-art infrastructure for professional aspirants hailing from both rural and urban areas.
- To impart technical education that encourages independent thinking, develops strong domain of knowledge, contemporary skills and positive attitudes towards holistic growth of young minds.

QUALITY POLICY

Sri Venkateswara College of Engineering and Technology strides towards excellence by adopting a system of quality policies and processes with continued improvements to enhance student's skills and talent for their exemplary contribution to the society, the nation and the world.

SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY
(AUTONOMOUS)
(AFFILIATED TO JNTUA, ANANTAPUR)

ACADEMIC REGULATIONS – R25

MASTER OF TECHNOLOGY (M. TECH)

REGULAR (Full-Time) TWO YEAR POST GRADUATE DEGREE PROGRAMME

(Effective for the students admitted into I year from the Academic Year 2025-26 and onwards)

Sri Venkateswara College of Engineering and Technology (Autonomous), offers **Two** Years (Four Semesters) full-time Master of Technology (M.Tech.) Degree programme, under Choice Based Credit System (CBCS) in different branches of Engineering and Technology with different specializations.

The Jawaharlal Nehru Technological University Anantapur, Ananthapuramu shall confer M.Tech Post Graduate degree to candidates who are admitted to the Master of Technology Program and fulfill all the requirements for the award of the degree.

1. **Applicability** :
   All the rules specified herein, approved by the Academic Council, shall be in the force and applicable to the students admitted from the Academic Year 2025-2026 onwards. Any reference to "College" in these rules and regulations stands for SVCET.

2. **Extent**: All the rules and regulations, specified hereinafter shall be read as a whole for the purpose of interpretation. As and when a doubt arises, the interpretation of the Chairman, Academic Council shall be final and ratified by the Academic Council in the forthcoming meeting. As per the requirements of statutory bodies, Principal, Sri Venkateswara College of Engineering College shall be the Chairman, Academic Council.

3. **Award of the M.Tech. Degree**
   A student will be declared eligible for the award of the M. Tech. degree if he/ she fulfils the following:
   - **3.1** Pursues a course of study for not less than two academic years and not more than four academic years.
   - **3.2** Registers for 75 credits and secures all 75 credits.

4 Students, who fail to fulfil all the academic requirements for the award of the degree within four academic years from the year of their admission, shall forfeit their seat in M. Tech. course and their admission stands cancelled.

5 **Programme of Study:**
The following M. Tech. Specializations are offered at present in different branches of Engineering and Technology in the institution:

Sl. No.	Discipline	Name of the Specialization	Code
01	Civil Engineering	Structural Engineering	20
02	Electrical and	Power Electronics & Electrical	54

	Electronics Engineering	Drives	
03	Mechanical Engineering	CAD / CAM	04
04	Electronics and Communication Engineering	VLSI Design	57
05	Computer Science and Engineering	Computer Science & Engineering	58
06		Data Science	32

and any other specializations as approved by AICTE/University from time to time.

6 Eligibility for Admissions:

6.1 Admission to the M. Tech Program shall be made subject to the eligibility, qualification and specialization prescribed by the A.P. State Government/University from time to time.

6.2 Admissions shall be made either on the basis of either the merit rank or Percentile obtained by the qualified student in the relevant qualifying GATE Examination/ the merit rank obtained by the qualified student in an entrance test conducted by A.P. State Government (APPGECET) for M. Tech. programmes/an entrance test conducted by University/on the basis of any other exams approved by the University, subject to reservations as laid down by the Govt. from time to time.

7 Programme related terms:

7.1 ***Credit:*** A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (Lecture/Tutorial) or two hours of practical work/field work per week.

Credit definition:

1 Hr. Lecture (L) per week	1 credit
1 Hr. Tutorial (T) per week	1 credit
1 Hr. Practical (P) per week	0.5 credit

7.2 Academic Year: Two consecutive (one odd + one even) semesters constitute one academic year.

7.3 Choice Based Credit System (CBCS): The CBCS provides choice for students to select from the prescribed courses.

8 Programme Pattern:

8.1 Total duration of the of M. Tech. programme is two academic years

8.2 Each academic year of study is divided into two semesters.

8.3 Each Semester shall be of 22 weeks duration (inclusive of Examinations), with a minimum of 90 instructional days per semester.

8.4 The student shall not take more than four academic years to fulfill all the academic requirements for the award of M. Tech. degree from the date of commencement of first year first semester, failing which the student shall forfeit the seat in M. Tech. programme.

8.5 The medium of instruction of the programme (including examinations

and project reports) will be in English only.

8.6 All subjects/courses offered for the M. Tech. degree programme are broadly classified as follows:

S. No.	Broad Course Classification	Course Category	Description
1.	Core Courses	Foundational & Professional Core Courses (PC)	Includes subjects related to the parent discipline / department / branch of Engineering
2.	Elective Courses	Professional Elective Courses (PE)	Includes elective subjects related to the parent discipline/ department/ branch of Engineering
		Open Elective Courses (OE)	Elective subjects which include inter-disciplinary subjects or subjects in an area outside the parent discipline which are of importance in the context of special skill development
3.	Research	Research methodology & IPR	To understand importance and process of creation of patents through research
		Technical Seminar	Ensures preparedness of students to undertake major projects / Dissertation, based on core contents related to specialization
		Cocurricular Activities	Attending conferences, scientific presentations and other scholarly activities
		Dissertation	M. Tech. Project or Major Project
4.	Audit Courses	Mandatory noncredit courses	Covering subjects of developing desired attitude among the learners is on the line of initiatives such as Unnat Bharat Abhiyan, Yoga, Value education etc.

8.7 The college shall take measures to implement Virtual Labs (https://www.vlab.co.in) which provide remote access to labs in various disciplines of Engineering and will help student in learning basic and advanced concept through remote experimentation. Student shall be made to work on virtual lab experiments during the regular labs.

8.8 A faculty advisor/mentor shall be assigned to each specialization to advise students on the programme, its Course Structure and Curriculum, Choice of Courses, based on his competence, progress, pre-requisites and interest.

8.9 Preferably 25% course work for the theory courses in every semester shall be conducted in the blended mode of learning.

9 Attendance Requirements:

9.1 A student shall be eligible to appear for the external examinations if he/she acquires i) a minimum of 50% attendance in each course and ii) 75% of attendance in aggregate of all the courses.

9.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester may be granted by the College Academic Committee.

9.3 Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representation by the candidate with supporting evidence

9.4 Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examination of that class.

9.5 A stipulated fee shall be payable towards condonation of shortage of attendance.

9.6 A student will not be promoted to the next semester unless he satisfies the attendance requirements of the present semester. They may seek re-admission into that semester when offered next.

9.7 If any candidate fulfils the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.

9.8 If the learning is carried out in blended mode (both offline & online), then the total attendance of the student shall be calculated considering the offline and online attendance of the student.

10 Evaluation – Distribution and Weightage of Marks:

The performance of a student in each semester shall be evaluated subject - wise (irrespective of credits assigned), for a maximum of 100 marks for theory and 100 marks forpractical, based on Internal Evaluation and End Semester Examination.

10.1 There shall be five units in each of the theory subjects. For the theory subjects 60 marks will be for the End Examination and 40 marks will be for Internal Evaluation.

10.2 Two Internal Examinations shall be conducted for 30 marks each, one in the middle of the Semester and the other immediately after the completion of instruction. First mid examination shall be conducted for I & II units of the syllabus and second mid examination for III, IV & V units. Each mid exam shall be conducted for a total duration of 120 minutes with 3 questions (without choice) each question for 10 marks. Final Internal marks for a total of 30 marks shall be arrived at by considering the marks secured by the student in both the internal examinations with 80% weightage to the better internal exam and 20% to the other. There shall be an online examination (TWO) conducted during the respective mid examinations by the college for the remaining 10 marks with 20 objective questions.

10.3 The following pattern shall be followed in the End Examination:

10.3.1 Five questions shall be set from each of the five units with either/or type for 12 marks each.

10.3.2 All the questions have to be answered compulsorily.

10.3.3 Each question may consist of one, two or more bits.

10.4 For practical subjects, 60 marks shall be for the End Semester Examinations and 40 marks will be for internal evaluation based on the day-to-day performance.
The internal evaluation based on the day-to-day work-10 marks, record-10 marks and the remaining 20 marks to be awarded by conducting an internal laboratory test. The end examination shall be conducted by the examiners, with a breakup mark of Procedure-10, Experimentation-25, Results-10, Viva- voce-15.

10.5 There shall be a Comprehensive Viva-Voce in I year – II sem for 2 credits. The Comprehensive Viva-Voce will be conducted by the committee consisting of Head of the Department and two senior faculty members of the department nominated by the Principal as recommended by the chairman, BOS. The Comprehensive Viva – Voce is aimed to assess the students understanding in various subjects he studies during the M. Tech I year course of study. The Comprehensive Viva – Voce shall be evaluated for 100 marks by the committee. There are no internal marks for the Comprehensive Viva – Voce. A student shall acquire 2 credits assigned to the Comprehensive Viva – Voce only when he secures 40% or more marks. In case, if a student fails in Comprehensive Viva – voce, he shall reappear as and when I/II supplementary examinations are conducted.

10.6 There shall be Mandatory **Audit courses** in I & II semesters for zero credits. There is no external examination for audit courses. However, attendance shall be considered while calculating aggregate attendance and student shall be declared to have passed the mandatory course only when he/she secures 50% or more in the internal examinations. In case, the student fails, a re- examination shall be conducted for failed candidates for 40 marks every six months/semester satisfying the conditions mentioned in item 1 & 2 of the regulations.

10.7 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

10.8 In case the candidate does not secure the minimum academic requirement in any of the subjects he/she has to reappear for the Semester Examination either supplementary or regular in that subject or repeat the course when next offered or do any other specified subject as may be required.

10.9 The laboratory records and mid semester test papers shall be preserved for a minimum of 3 years in the respective institutions as per the University norms and shall be produced to the Committees of the University as and when the same are asked for.

10.10 Industry internship with a minimum of eight weeks duration, done at the end of second semester. The internship can be done by the students at local industries, Govt. Organizations, construction agencies, Industries, Hydel and thermal power projects and also in software MNCs. Evaluation of the industry internship shall be through the departmental committee. A student will be required to submit industry internship report to the concerned department and appear for an oral presentation before the

departmental committee. The report and the oral presentation shall carry 40% and 60% weightages respectively. A student shall acquire 2 credits assigned to the industry internship only when he secures 40% or more marks. In case, if a student fails in industry internship, he shall reappear as and when II/III supplementary examinations are conducted.

11 Credit Transfer Policy

As per University Grants Commission (Credit Framework for Online Learning Courses through SWAYAM) Regulation, 2016, the Institution shall allow up to a maximum of 40% of the total courses being offered in a particular Programme in a semester through the Online Learning courses through SWAYAM.

11.1 The Institution shall offer credit mobility for MOOCs and give the equivalent credit weightage to the students for the credits earned through online learning courses through SWAYAM platform.

11.2 The online learning courses available on the SWAYAM platform will be considered for credit transfer. SWAYAM course credits are as specified in the platform

11.3 Student registration for the MOOCs shall be only through the institution, it is mandatory for the student to share necessary information with the institution

11.4 The institution shall select the courses to be permitted for credit transfer through SWAYAM. However, while selecting courses in the online platform institution would essentially avoid the courses offered through the curriculum in the offline mode.

11.5 The institution shall notify at the beginning of semester the list of the online learning courses eligible for credit transfer in the forthcoming Semester.

11.6 The institution shall also ensure that the student has to complete the course and produce the course completion certificate as per the academic schedule given for the regular courses in that semester

11.7 The institution shall designate a faculty member as a Mentor for each course to guide the students from registration till completion of the credit course.

11.8 The Institution shall ensure no overlap of SWAYAM MOOC exams with that of the Internal / External examination schedule. In case of delay in SWAYAM results, the Institution will re-issue the marks sheet for such students.

11.9 Student pursuing courses under MOOCs shall acquire the required credits only after successful completion of the course and submitting a certificate issued by the competent authority along with the percentage of marks and grades.

11.10 The departments shall submit the following to the examination section of the Institution:

a) List of students who have passed MOOC courses in the current semester along with the certificates of completion.
b) Undertaking form filled by the students for credit transfer.

11.11 The Institution shall resolve any issues that may arise in the implementation of this policy from time to time and shall review its

credit transfer policy in the light of periodic changes brought by UGC, SWAYAM, NPTEL and state government.

Note: Students shall also be permitted to register for MOOCs offered through online platforms other than SWAYAM NPTEL. In such cases, credit transfer shall be permitted only after seeking approval of the Head of the Institution at least three months prior to the commencement of the semester.

12 Re-registration for Improvement of Internal Evaluation Marks:

A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and has failed in the end examination

12.1 The candidate should have completed the course work and obtained examinations results for **I, II and III** semesters.

12.2 The candidate should have passed all the subjects for which the Internal Evaluation marks secured are more than 50%.

12.3 Out of the subjects the candidate has failed in the examination due to Internal Evaluation marks secured being less than 50%, the candidate shall be given one chance for each Theory subject and for a maximum of **three** Theory subjects for Improvement of Internal evaluation marks.

12.4 The candidate has to re-register for the chosen subjects and fulfill the academic requirements.

12.5 For reregistration the candidates have to submit the applications to the Head of the Institution through the Head of the Department by paying the requisite fees (For each course, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the amount is to be remitted in the form of D.D./ Challan in favour of the Principal, Sri Venkateswara College of Engineering & Technology) and get approval from the Head of the Institution before the start of the semester in which re-registration is required.

12.6 In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

13 Evaluation of Project/Dissertation Work:

The Project work shall be initiated at the beginning of the III Semester and the duration of the Project is of two semesters. Evaluation of Project work is for 300 marks with 200 marks for internal evaluation and 100 marks for external evaluation. Internal evaluation of the Project Work – I & Project work – II in III & IV semesters respectively shall be for 100 marks each. External evaluation of final Project work viva voce in IV semester shall be for 100 marks.

A Project Review Committee (PRC) shall be constituted with the Head of the Department as Chairperson, Project Supervisor and one faculty member of the department offering the M.Tech. programme.

13.1 A candidate is permitted to register for the Project Work in III

Semester after satisfying the attendance requirement in all the subjects, both theory and laboratory (in I & II semesters).

13.2 A candidate is permitted to submit Project dissertation with the approval of PRC. The candidate has to pass all the theory, practical and other courses before submission of the Thesis.

13.3 Project work shall be carried out under the supervision of teacher in the parent department concerned.

13.4 A candidate shall be permitted to work on the project in an industry/research organization on the recommendation of the Head of the Department. In such cases,one of the teachers from the department concerned would be the internal guide and an expert from the industry/ research organization concerned shall act as co-supervisor/ external guide. It is mandatory for the candidate to make full disclosure of all data/results on which they wish to base their dissertation. They cannot claim confidentiality simply because it would come into conflict with the Industry"s or R&D laboratory"s own interests. A certificate from the external supervisor is to be included in the dissertation.

13.5 Continuous assessment of Project Work - I and Project Work – II in III & IV semesters respectively will be monitored by the PRC.

13.6 The candidate shall submit status report by giving seminars in three different phases (two in III semester and one in IV semester) during the project work period. These seminar reports must be approved by the PRC before submission of the Project Thesis.

13.7 After registration, a candidate must present in Project Work Review - I, in consultation with his Project Supervisor, the title, objective and plan of action of his Project work to the PRC for approval within four weeks from the commencement of III Semester. Only after obtaining the approval of the PRC can the student initiate the project work.

13.8 The Project Work Review - II in III semester carries internal marks of 100. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate the work for the other 50 marks. The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Project Work.

13.9 A candidate has to secure a minimum of 50% of marks to be declared successful in Project Work Review - II. Only after successful completion of Project Work Review – II, candidate shall be permitted for Project Work Review – III in IV Semester. The unsuccessful students in Project Work Review - II shall reappear for it as and when supplementary examinations are conducted.

13.10 The Project Work Review - III in IV semester carries 100 internal marks. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The PRC will examine the overall progress of the Project Work and decide whether or not eligible for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Project Work Review - III. If he fails to obtain the required minimum marks, he has to reappear for Project Work Review - III after a month.

13.11 For the approval of PRC the candidate shall submit the draft copy of dissertation to the Head of the Department and make an oral

presentation before the PRC.

13.12 After approval from the PRC, the students are required to submit a report showing that the plagiarism is within 30%. The dissertation report will be accepted only when the plagiarism is within 30%, which shall be submitted along with the dissertation report.

13.13 Research paper related to the Project Work shall be published in conference proceedings/UGC recognized journal. A copy of the published research paper shall be attached to the dissertation.

13.14 After successful plagiarism check and publication of research paper, three copies of the dissertation certified by the supervisor and HOD shall be submitted to the College.

13.15 The dissertation shall be adjudicated by an external examiner selected by the Head of the Institution. For this, the supervisor concerned and department head for each student shall submit a panel of three examiners to the Principal. However, the dissertation will be adjudicated by one examiner nominated by the Head of the Institution.

13.16 If the report of the examiner is not satisfactory, the candidate shall revise and resubmit the dissertation, in the time frame as decided by the PRC. If report of the examiner is unfavorable again, the thesis shall be summarily rejected. The candidate has to reregister for the project and complete the project within the stipulated time after taking the approval from the Head of the Institution

13.17 If the report of the examiner is satisfactory, the Head of the Department shall coordinate and make arrangements for the conduct of Project Viva voce exam.

13.18 The Project Viva voce examinations shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who has adjudicated the dissertation. For Dissertation Evaluation (Viva voce) in IV Sem. there are external marks of 100 and it is evaluated by external examiner. The candidate has to secure a minimum of 50% marks in Viva voce exam.

13.19 If he fails to fulfill the requirements as specified, he will reappear for the Project Viva voce examination only after three months. In the reappeared examination also, if he fails to fulfill the requirements, he will not be eligible for the award of the degree.

14 Credits for Co-curricular Activities

The credits assigned for co-curricular activities shall be given by the Head of the Department and the same shall be submitted to the Examination section through Head of the Institution.

A Student shall earn 01 credit under the head of co-curricular activities, viz., attending Conference, Scientific Presentations and Other Scholarly Activities.

Following are the guidelines for awarding Credits for Co-curricular Activities

Name of the Activity	Maximum Credits / Activity

Participation in National Level Seminar/ Conference / Workshop /Training programs (related to the specialization of the student)	1
Participation in International Level Seminar / Conference / workshop/Training programs held outside India (related to the specialization of the student)	1
Academic Award/Research Award from State Level/National Agencies	1
Academic Award/Research Award from International Agencies	1
Research / Review Publication in National Journals (Indexed in Scopus / Web of Science)	1
Research / Review Publication in International Journals with Editorial board outside India (Indexed in Scopus / Web of Science)	1

Note:

i) Credit shall be awarded only for the first author. Certificate of attendance and participation in a Conference/Seminar is to be submitted for awarding credit.

ii) Certificate of attendance and participation in workshops and training programs (Internal or External) is to be submitted for awarding credit. The total duration should be at least one week.

iii) Participation in any activity shall be permitted only once for acquiring required credits under cocurricular activities

15. Results Committee

Results Committee comprising of Principal, Controller of Examinations, Additional Controller of Examinations, One Senior Professor nominated by the Principal, and the University Nominee will oversee the details of marks, grades, and pass percentages of all the subjects and branch-wise pass percentages.

Office of the Controller of Examinations will generate student-wise result sheets and the same will be published through the college website.

Student-wise Grade Sheets are generated and issued to the students.

16 Grading:

As a measure of the student"s performance, a 10-point Absolute Grading System using the following Letter Grades and corresponding percentage of marks shall be followed:

After each course is evaluated for 100 marks, the marks obtained in each course will be converted to a corresponding letter grade as given

below, depending on the range in which the marks obtained by the student fall.

Structure of Grading of Academic Performance

Range in which the marks in the subject fall	Grade	Grade points Assigned
≥ 90	S (Superior)	10
≥ 80 < 90	A (Excellent)	9
≥ 70 < 80	B (Very Good)	8
≥ 60 < 70	C (Good)	7
≥ 50 < 60	D (Pass)	6
< 50	F (Fail)	0
Absent	Ab (Absent)	0

i) A student obtaining Grade „F" or Grade „Ab" in a subject shall be considered failed and will be required to reappear for that subject when it is offered the next supplementary examination.
ii) For noncredit audit courses, "Satisfactory" or "Unsatisfactory" shall be indicated instead of the letter grade and this will not be counted for the computation of SGPA/CGPA/Percentage.

Computation of Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):

The Semester Grade Point Average (SGPA) is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e.,

$$SGPA = \Sigma (C_i \times G_i)/\Sigma C_i$$

where, C_i is the number of credits of the i^{th} subject and G_i is the grade point scored by the student in the i^{th} course.

i) The Cumulative Grade Point Average (CGPA) will be computed in the same manner considering all the courses undergone by a student over all the semesters of a program, i.e.,

$$CGPA = \Sigma (C_i \times S_i)/ \Sigma C_i$$

where "S_i" is the SGPA of the i^{th} semester and C_i is the total number of credits up to that semester.
ii) Both SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.
iii) While computing the SGPA the subjects in which the student is awarded Zero grade points will also be included.

Grade Point: It is a numerical weight allotted to each letter grade on a 10-point scale. Letter Grade: It is an index of the performance of students in a said course. Grades are denoted by letters S, A, B, C, D and F.

17. Personal Verification / Revaluation / Final Valuation

17.1 Personal Verification of Answer Scripts:

Candidates appear in a particular semester end examinations may appeal for verification of their answer script(s) for arithmetic correction in totaling of marks and any omission / deletion in evaluation within 7 days from the date of declaration of results at the office of the Controller of Examinations on the prescribed proforma and by paying the prescribed fee per answer script.

It is clarified that personal verification of answer script shall not tantamount to revaluation of answer script. This is only a process of reverification by the candidate. Any mistake / deficiency with regard to arithmetic correction in totaling of marks and any omission / deletion in evaluation if found, the institution will correct the same.

17.2 Recounting / Revaluation:

Students shall be permitted for request for recounting/revaluation of the Semester-End examination answer scripts within a stipulated period after payment of prescribed fee. After recounting or revaluation, records are updated with changes if any and the student will be issued a revised grade sheet. If there are no changes, the same will be intimated to the students.

17.3 Final Valuation:

Students shall be permitted for request for final valuation of the Semester–End Examination answer scripts within a stipulated period after the publication of the revaluation results by paying the necessary fee. The final valuation shall be carried out by an expert not less than Associate Professor as per the scheme of valuation supplied by the examination branch in the presence of the student, Controller of Examinations and Principal. However students are not permitted to discuss / argue with the examiner. If the increase in marks after final valuation is equal to or more than 15% of the previous valuation marks, the marks obtained after final valuation shall be treated as final. If the variation of marks after final valuation is less than 15% of the previous valuation marks, then the earlier valuation marks shall be treated as the final marks.

17.4 Supplementary Examinations: In addition to the regular semester-end examinations conducted, the College may also schedule and conduct supplementary examinations for all the courses of other semesters when feasible for the benefit of students. Such of the candidates writing supplementary examinations may have to write more than one examination per day.

18. Award of Class:

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following three classes:

Class Awarded	Cumulative Grade Point Average
First Class with Distinction	≥7.75

First Class	≥6.75 and<7.75
Second Class	≥6.0 and <6.75

19. Exit Policy: The student shall be permitted to exit with a PG Diploma based on his/her request to the Head of the Institution through the respective Head of the Department at the end of first year subject to passing all the courses in first year.

The Head of the Institution shall resolve any issues that may arise in the implementation of this policy from time to time and shall review the policy in the light of periodic changes brought by UGC, AICTE, Affiliating University and State government.

20. Withholding of Results:

If the candidate has any case of in-discipline pending against him, the result of the candidate shall be withheld, and he will not be allowed/promoted into the next higher semester. The issue of degree is liable to be withheld in such cases.

20. Transitory Regulations

Discontinued, detained, or failed candidates are eligible for readmission as and when the semester is offered after fulfilment of academic regulations. Candidates who have been detained for want of attendance or not fulfilled academic requirements or who have failed after having undergone the course in earlier regulations or have discontinued and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when subjects are offered, subject to Section 2 and they will follow the academic regulations into which they are readmitted.

21. Medium of Instruction:

The Medium of Instruction is English for all courses, laboratories, Internal and External examinations, Seminar Presentation and Project Reports.

22. Mode of Learning:

Preferably 50% course work for the theory courses in every semester shall be conducted in the blended mode of learning. If the blended learning is carried out in online mode, then the total attendance of the student shall be calculated considering the offline and online attendance of the student.

23. General Instructions:

23.1 The academic regulations should be read as a whole for purpose of any interpretation.

23.2 Disciplinary action for Malpractice/improper conduct in examinations is appended.

23.3 There shall be no places transfer within the constituent colleges and affiliated colleges of Jawaharlal Nehru Technological University Anantapur.

23.4 Where the words "he", "him", "his", occur in the regulations, they

include “she”, “her”, “hers”.

23.5 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.

23.6 The University / Institution may change or amend the academic regulations or syllabi at any time and the changes or amendments shall be made applicable to all the students on rolls with effect from the dates notified by the University / Institution.

23.7 The above rules and regulations are to be approved / ratified by the College Academic Council as and when any modification is to be done.

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Identification of Courses

M. Tech

Each course shall be uniquely identified by an alphanumeric code of width 7 characters as given below.

No. of Digits	Description
First two digits	Year of regulations Ex:25
Next one letter	Type of program: A: B. Tech B: M. Tech C: M.B.A D: M.C.A E: BBA F: BCA
Next two letters	Code of program: ST: Structural Engineering, P.E: Power Electronics & Electric Drives, CM: CAD/CAM, VL: VLSI, CS: Computer Science and Engineering, DS: Data Science
Last two digits	Indicate serial numbers: ≥ 01

Ex:
25BST01
25BPE01
25BCM01
25BVL01
25BCS01
25BDS01
25BMB01
25BHS01

SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY
(AUTONOMOUS)
(AFFILIATED TO JNTUA, ANANTHAPURAMU)
RULES FOR DISCIPLINARY ACTION FOR MALPRACTICE / IMPROPER CONDUCT IN EXAMINATIONS

Sl.No.	Nature of Malpractices / Improper conduct If the candidate	Punishment
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination).	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester / year. The Hall Ticket of the candidate is to be cancelled.
3.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and

		project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester / year.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that Semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that Semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
6.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that Semester/year. The candidate is also debarred and forfeits of seat.
7.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and

		forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practical"s and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the impostor is an outsider, he will be handed over to the police and a case is registered against him.
8.	Refuses to obey the orders of the Chief Superintendent / Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in-charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction or property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate (s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester / year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.

	to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester / year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the Examination committee for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.

Note:

Whenever the performance of a student is cancelled in any subject/subjects due to Malpractice, he has to register for End Examinations in that subject/subjects consequently and has to fulfil all the norms required for the award of Degree.

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Department Vision & Mission under R-25 Regulations

VISION

To become a centre of excellence in the field of electronics and communications offering higher order of learning and conducting contemporary research thereby producing globally competitive and ethically strong engineering professionals.

MISSION

- Establish a scintillating learning environment to produce quality graduates with passion for knowledge and creativity in the field of Electronics and Communication Engineering.
- Impart quality education through periodically updated curriculum to meet the challenges of the industry and research at the global level.
- Enhancing employability of the students by providing skills through comprehensive experiential learning.
- Developing professional etiquette and ethical integrity among the students to face real-time life challenges.
- Empower the faculty through continuous training in domain, research and pedagogy for enhancing learning outcomes of the students and Research output.

Program Education Objectives (PEOs)

PEO1:

Identify and apply appropriate Electronic Design Automation (EDA) to solve real world problems in VLSI domain to create innovative products and systems.

PEO2:

Develop managerial skill and apply appropriate approaches in the domains of VLSI design incorporating safety, sustainability and become a successful professional or an Entrepreneur in the domain.

PEO3:

Pursue career in research in VLSI Design domain through self learning and self directed on cutting edge technologies.

Program Outcomes of M.Tech-VLSI Design

PO1: Independently carry out research /investigation and development work to solve practical problems related to VLSI Design.

PO2: Write and present a substantial technical report/document in the field of VLSI Design.

PO3: Demonstrate a degree of mastery over the areas of VLSI Design. The mastery should be at a level higher than the requirements in the bachelor's in Electronics & Communication Engineering.

PO4: Propose and execute optimal solutions for problems in the field of VLSI design.

PO5: Apply appropriate methodology and modern engineering/IT tools to meet the international standards in the area of VLSI design.

PO6: Acquire integrity and ethics of research to execute projects efficiently.

Program Specific Outcomes of M.Tech-VLSI Design

PSO1: Acquire competency in areas of VLSI, IC Fabrication, Design, Testing, Verification and prototype development focusing on applications.

PSO2: An exposure to variety of programming languages and software's.

SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY
(AUTONOMOUS)
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Course Structure and Scheme of Examination for M.Tech –VLSI Design under Academic Regulations R-25

M.Tech I- Semester **Regulations: R25**

S. No	Category	Course Code	Course Name	Hours/week			Credits	Scheme of Examination Maximum Marks		
				L	T	P	C	CIA	SEE	Total
1	PC	25BVL01	CMOS Analog IC Design	3	0	0	3	40	60	100
2	PC	25BVL02	CMOS Digital IC Design	3	0	0	3	40	60	100
3	PE		**Professional Elective – I**	3	0	0	3	40	60	100
		25BVL03	Microchip Fabrication Techniques							
		25BVL04	Scripting Languages for VLSI							
		25BVL05	CAD for VLSI							
4	PE		**Professional Elective – II**	3	0	0	3	40	60	100
		25BVL06	Device Modelling							
		25BVL07	FPGA Architectures and Applications							
		25BVL08	ASIC Design							
5	PC	25BVL09	CMOS Analog IC Design Lab	0	0	4	2	40	60	100
6	PC	25BVL10	CMOS Digital IC Design Lab	0	0	4	2	40	60	100
7	MC	25BMB01	Research Methodology and IPR	2	0	0	2	40	60	100
8	SC	25BVL11	RTL Synthesis, Simulation and verification	0	1	2	2	40	60	100
9	AC		**Audit Course –I**	2	0	0	0	-	-	-
		25BHS04	English for Research paper writing							
		25BST11	Disaster Management							
		25BHS05	Essence of Indian Traditional Knowledge							
TOTAL				**16**	**1**	**10**	**20**	**320**	**480**	**800**

M.Tech II- Semester **Regulations: R25**

S. No	Category	Course Code	Course Name	Hours/week			Credits	Scheme of Examination Maximum Marks		
				L	T	P	C	CIA	SEE	Total
1	PC	25BVL12	CMOS Mixed Signal IC Design	3	0	0	3	40	60	100
2	PC	25BVL13	Physical Design Automation	3	0	0	3	40	60	100
3	PE		**Professional Elective – III**	3	0	0	3	40	60	100
		25BVL14	SoC Testing and Verification							
		25BVL15	Semiconductor Memory Design and Testing							
		25BVL16	Advanced VLSI interconnects							
4	PE		**Professional Elective – IV**	3	0	0	3	40	60	100
		25BVL17	Low Power VLSI Design							
		25BVL18	Algorithms for VLSI Design							
		25BVL19	VLSI Signal Processing							
5	PC	25BVL20	CMOS Mixed Signal IC Design Lab	0	0	4	2	40	60	100
6	PC	25BVL21	Physical Design Automation Lab	0	0	4	2	40	60	100
7	MC	25BCS22	Quantum Technologies and Applications	2	0	0	2	40	60	100
8	PC	25BVL22	Comprehensive Viva Voce	0	0	0	2		100	100
9	AC		**Audit Course – II**	2	0	0	0	-	-	-
		25BMB02	Pedagogy Studies							
		25BHS06	Yoga for Stress Management							
		25BHS07	Personality Development through Life Enlightenment Skills							
TOTAL				**16**	**0**	**8**	**20**	**280**	**520**	**800**

SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY
(AUTONOMOUS)
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Course Structure and Scheme of Examination for M.Tech –VLSI Design under Academic Regulations R-25

M.Tech III- Semester **Regulations: R25**

S. No	Category	Course Code	Course Name	Hours/week			Credits	Scheme of Examination Maximum Marks		
				L	T	P	C	CIA	SEE	Total
1	PE	25BVL23	**Professional Elective – V** Bi-CMOS Technology and Applications	3	0	0	3	40	60	100
		25BVL24	Optimization Techniques and Applications in VLSI Design							
		25BVL25	SoC Architecture							
2	OE	25BCM26	**Open Elective-I** IoT and its Applications	3	0	0	3	40	60	100
		25BCS01	Advanced data structures & Algorithms							
		25BCS04	Cloud Computing							
3	PR	25BVL27	Dissertation Phase – I	0	0	20	10	40	60	100
4	PC	25BVL28	Industry Internship	0	0	0	2		100	100
5	PC	25BVL29	Co-curricular Activities	0	0	0	1	-	-	-
TOTAL				**6**	**0**	**20**	**19**	**120**	**280**	**400**

M.Tech IV- Semester **Regulations: R25**

S. No	Category	Course Code	Course Name	Hours/week			Credits	Scheme of Examination Maximum Marks		
				L	T	P	C	CIA	SEE	Total
1	PR	25BVL30	Dissertation Phase – II	0	0	32		120	180	300
TOTAL				0	0	32		120	180	300

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS)

M.Tech-I Semester-VLSI Design

Course Code: 25BVL01

CMOS ANALOG IC DESIGN

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Design MOSFET based analog integrated circuits.

CO2: Analyze analog circuits at least to the first order.

CO3: Appreciate the trade-offs involved in analog integrated circuit design.

CO4: Understand and appreciate the importance of noise and distortion in analog circuits.

CO5: Analyze complex engineering problems critically in the domain of analog IC design for conducting research.

CO6: Solve engineering problems for feasible and optimal solutions in the core area

UNIT-I:

Basic MOS Device Physics: General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models and MOS Capacitor. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.

UNIT-II:

Differential Amplifiers: Single Ended and Differential Operation, Basic Differential Pair, Common Mode Response, Differential Pair with MOS loads, Gilbert Cell. Passive and Active Current Mirrors – Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors. Current Steering Circuit.

UNIT-III:

Frequency Response of Amplifiers: General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.

UNIT-IV:

Feedback Amplifiers: General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op

Amps, Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps, Stability and Frequency Compensation.

UNIT-V:

Operational Amplifiers: One Stage Op-Amp, Two Stage Op-Amp, Gain Boosting, Common Mode Feed-Back, Input Range Limitations, Slew Rate, PSRR. Compensation of Two Stage Op-Amp, Slewing in Two Stage Op-Amp, Compensation Techniques. Design Procedure for 2-Stage Op-Amp.

Text Books:

1. B.Razavi, "Design of Analog CMOS Integrated Circuits", 2ndEdition, McGraw Hill Edition2016.

2. Paul.R.Gray& Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley**,** 5thEdition, 2009.

Reference Books:

1. T.C.Carusone, D.A.Johns&K.Martin, "Analog Integrated Circuit Design", 2ndEdition, Wiley, 2012.

2. P.E.Allen&D.R.Holberg, "CMOS Analog Circuit Design", 3rd Edition, Oxford University Press, 2011.

3. R.Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rdEdition, Wiley, 2010.

4. Adel S. Sedra, Kenneth C. Smith, Arun, "Microelectronic Circuits", 6thEdition, Oxford University Press

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS)

M.Tech-I Semester-VLSI Design

Course Code: 25BVL02

CMOS DIGITAL IC DESIGN

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS,

CO2: Estimate Delay and Power of Adders circuits.

CO3: Classify different semiconductor memories.

CO4: Analyze, design and implement combinational and sequential MOS logic circuits.

CO5: Analyze complex engineering problems critically in the domain of digital IC design for conducting research.

CO6: Solve engineering problems for feasible and optimal solutions in the core area of digital ICs

UNIT-I:

MOS Design Pseudo NMOS Logic: Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II:

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR & NAND gate, Complex Logic circuits design–Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT-III:

Sequential MOS Logic Circuits: Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT-IV:

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT-V:

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

Text Books:

1. Neil Weste, David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Pearson, 2010
2. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
3. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Edition, 2011.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M.Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2ndEdition, PHI.

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS)

M.Tech-I Semester-VLSI Design

Course Code: 25BVL03

MICROCHIP FABRICATION TECHNIQUES
(PROFESSIONAL ELECTIVE – I)

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Understand various stages of fabrication

CO2: Understand Various packaging techniques and Design rules.

CO3: Classify various thin films and its characteristics

UNIT – I:

Introduction to Processing: Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Yield measurement, Contamination sources, Clean room construction.

UNIT – II:

Photolithography: Oxidation and Photolithography, Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping.

UNIT – III:

Diffusion & Ion Implantation: Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2.

UNIT – IV:

Film Depositions and Growth: Metallization, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy.

UNIT – V:

Yield: Design rules and Scaling, BICMOS ICs: Choice of transistor types, PNP transistors, Resistors, capacitors.

Packaging: Chip characteristics, package functions, package operations.

Text Books:

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 1997.
2. Plummer, J.D., Deal, M.D. and Griffin, P.B., "Silicon VLSI Technology: Fundamentals, Practice and Modeling", 3rd Ed., Prentice-Hall, 2000.

Reference Books:

1. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000.
2. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994.
3. S.M. Sze, VLSI technology, McGraw-Hill Book company, NY, 1988.

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-I Semester-VLSI Design

Course Code: 25BVL04

SCRIPTING LANGUAGES FOR VLSI
(PROFESSIONAL ELECTIVE – I)

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Gain fluency in programming with scripting languages

CO2: Create and run scripts using PERL/TCL/PYTHON in CAD Tools

CO3: Demonstrate the use of PERL/PYTHON/ TCL in developing system and web applications

CO4: Develop a real time project using PERL/PYTHON

UNIT – I:

Introduction to Scripts and Scripting: Basics of Linux, Origin of Scripting languages, scripting today, Characteristics and uses of scripting languages.

UNIT – II:

PERL: Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT – III:

Advanced PERL: Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects and modules in action, Tied variables, interfacing to the operating systems, Security issues.

UNIT – IV:

TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT – V:

Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, TCL and TK integration.

PYTHON: Introduction to PYTHON language, PYTHON-syntax, statements, functions, Built-in functions and Methods, Modules in PYTHON, Exception Handling.

Text Books:

1. The World of Scripting Languages- David Barron, Wiley Student Edition.
2. PYTHON Web Programming, Steve Holden and David Beazley, New Riders Publications.

Reference Books:

1. TCL/TK: A Developer's Guide- ClifFlynt, Morgan Kaufmann Series.
2. Core PYTHON Programming, Chun, Pearson Education.
3. Learning Perl, Randal L. Schwartz, O' Reilly publications 6th edition.
4. Linux: The Complete Reference", Richard Peterson McGraw Hill Publications, 6th Edition

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-I Semester-VLSI Design

Course Code: 25BVL05

CAD FOR VLSI
(PROFESSIONAL ELECTIVE – I)

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.

CO2: Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.

CO3: Practice the application of fundamentals of VLSI technologies

CO4: Optimize the implemented design for area, timing and power by applying suitable constraints.

UNIT-I:

Introduction: VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

UNIT-II:

Partitioning: Partitioning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing.

UNIT-III:

Floor Planning: Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments.

UNIT-IV:

Placement and Routing: Placement–Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.

Global Routing and Detailed Routing: Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

UNIT-V:

Physical Design Automation of FPGAs and MCMs: FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Introduction to MCM Technologies, MCM Physical Design Cycle.

Text Books:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani,3rdEdition, 2005, Springer International Edition.

2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

Reference Books:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.

2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.

3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-I Semester-VLSI Design

Course Code: 25BVL06

DEVICE MODELLING
(PROFESSIONAL ELECTIVE – II)

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Understand the physics of 2-terminal MOS operation and its characteristics

CO2: Understand the physics of 4-terminal MOSFET operation and its characteristics.

CO3: Analyze the SOI MOSFET electrical characteristics.

UNIT – I:

2-terminal MOS device: threshold voltage modelling (ideal case as well as considering the effects of Qf, Φms and Dit.).

UNIT – II:

C-V characteristics (ideal case as well as taking into account the effects of Qf, Φms and Dit): MOS capacitor as a diagnostic tool (measurement of non-uniform doping profile, estimation of Qf, Φms and Dit)

UNIT - III

4-terminal MOSFET: threshold voltage (considering the substrate bias); above threshold I-V modelling (SPICE level 1,2,3 and 4).

UNIT - IV

Sub threshold current model: scaling; effect of threshold tailoring implant (analytical modelling of threshold voltage using box approximation); buried channel MOSFET. Short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer's model)

UNIT – V:

SOI MOSFET: Basic structure; threshold voltage modelling Advanced topics: hot carriers in Channel; EEPROMs; CCDs; high-K gate dielectrics.

Text Books:

1. S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.

2. M. Lund strom, Fundamentals of Nano transistors, World Scientific Publishing Co Pte Ltd 2017.

Reference Books:

1. Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.

2. E. Takeda, Hot-carrier Effects in MOS Trasistors, Academic Press, 1995.

3. J. P. Colinge, “FinFETs and Other Multi-Gate Transistors,” Springer. 2009

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-I Semester-VLSI Design

Course Code: 25BVL07

FPGA ARCHITECTURES AND APPLICATIONS
(PROFESSIONAL ELECTIVE – II)

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Acquire knowledge about various architectures and device technologies of PLD's.

CO2: Comprehend FPGA Architectures.

CO3: Analyze System level Design and their application for Combinational and Sequential Circuits.

CO4: Familiarize with Anti-Fuse Programmed FPGAs.

CO5: Apply knowledge of this subject for various design applications.

UNIT – I:

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices– Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT – II:

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

UNIT – III:

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT – IV:

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT – V:

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture

Text Books:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.

2. Digital Systems Design - Charles H. Roth Jr, LizyKurian John, Cengage Learning.

Reference Books:

1. Field Programmable Gate Arrays-John V.Oldfield, Richard C.Dorf, Wiley India.

2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad, Pearson Low Price Edition.

3. Digital Systems Design with FPGAs and CPLDs-Ian Grout, Elsevier,Newnes.

4. FPGA based System Design-Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-I Semester-VLSI Design

Course Code: 25BVL08

ASIC DESIGN
(PROFESSIONAL ELECTIVE – II)

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Understand different types of ASICs and their libraries.

CO2: Understand about programmable ASICs, I/O modules and their interconnects.

CO3: Familiarize different methods of software ASIC design their simulation, testing and construction of ASICs.

UNIT – I:

Introduction to ASICs: Types of ASICs, Design Flow, Case Study, Economics of ASICs, ASIC Cell Libraries, Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Library Cell Design, Library Architecture, Gate-Array Design, Standard Cell Design, Data Path Cell Design.

UNIT – II:

Programmable ASICs and Programmable ASIC Logic Cells: The Anti fuse, Static Ram, EPROM and EEPROM Technology, Practical Issues, Specifications, PREDP Benchmarks, FPGA Economics, Actel ACT, Xilinx LCA, Altera Flex, Altera Max.

UNIT – III:

I/O Cells and Interconnects & Programmable ASIC Design Software: DC Output, AC Output, DC input, AC input, Clock input, Power input, Xilinx I/O block, Other I/O Cells, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera FLEX, Design Systems, Logic Synthesis, The Half gate ASIC.

UNIT – IV:

Low Level Design Entry and Logic Synthesis: Schematic Entry, Low level Design Languages, PLA Tools, EDIF, A logic synthesis example, A Comparator/MUX, Inside a Logic Synthesizer, Synthesis of Viterbi Decoder, Verilog and Logic synthesis, VHDL and Logic Synthesis, Finite State Machine Synthesis, Memory Synthesis, The Engine Controller, Performance Driven Synthesis, Optimization of the viter bi decoder.

UNIT – V:

Simulation, Test and ASIC Construction: Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch Level Simulation, Transistor Level Simulation, The importance of test, Boundary Scan Test, Faults, Faults Simulation, Automatic Test Pattern Generator, Scan Test, Built in Self-Test, A simple test Example, Physical Design, CAD Tools, System Partitioning, Estimating ASIC Size, Power Dissipation, FPGA Partitioning, Partitioning Methods.

Text Books:

1. Michael John Sebastian Smith, "Application Specific Integrated Circuits", Pearson Education, 2003.
2. L.J.Herbst, "Integrated Circuit Engineering", Oxford Science Publications, 1996.

Reference Books:

1. Himanshu Bhatnagar, "Advanced ASIC Chip Synthesis using Synopsis Design Compiler", 2nd Edition, Kluwer Academic, 2001.

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS)

M.Tech-I Semester-VLSI Design

Course Code: 25BVL09

CMOS ANALOG IC DESIGN LAB

L	T	P	C
0	0	4	2

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Explain the VLSI Design Methodologies using VLSI design tool.

CO2: Grasp the significance of various CMOS analog circuits in full-custom IC Design Flow.

CO3: Explain the Physical Verification in Layout Design

CO4: Fully appreciate the design and analyze of analog and mixed signal simulation

CO5: Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

List of Experiments:

The students are required to design and implement using CMOS 130nm Technology. The students are required to implement LAYOUTS of any **SIX** Experiments using CMOS 130nm Technology and Compare the results with Pre-Layout Simulation.

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. Simple current mirror
6. Cascode current mirror.
7. Wilson current mirror.
8. Differential Amplifier
9. Two stage Operational Amplifier
10. Sample and Hold Circuit
11. Direct-conversion ADC
12. R-2R Ladder Type DAC

Lab Requirements:

Software: Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-I Semester-VLSI Design

Course Code: 25BVL10

CMOS DIGITAL IC DESIGN LAB

L	T	P	C
0	0	4	2

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Explain the VLSI Design Methodologies using any VLSI design tool.

CO2: Grasp the significance of various design logic Circuits in full-custom IC Design.

CO3: Explain the Physical Verification in Layout Extraction.

CO4: Fully appreciate the design and analyze of CMOS Digital Circuits.

Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

LIST OF EXPERIMENTS

The students are required to design and implement the Circuit and Layout of any **TWELVE** Experiments using CMOS Technology.

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

Lab Requirements:

Software: Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software

Hardware: Personal Computer with necessary peripherals, configuration and operating System.

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-I Semester-VLSI Design

Course Code: 25BMB04

RESEARCH METHODOLOGY AND IPR
(MADATORY COURSE)

L	T	P	C
2	0	0	2

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Recall key concepts and terminology related to research design, data collection, and intellectual property rights.

CO2: Explain the importance of research design and data analysis in research studies, and describe the concept of intellectual property rights.

CO3: Design a research study, including data collection and analysis methods, and apply intellectual property rights principles to protect research findings.

CO4: Analyze research studies to identify strengths and limitations, and evaluate the effectiveness of data collection and analysis methods.

CO5: Assess the impact of intellectual property rights on research and innovation, and evaluate the effectiveness of research designs and methods.

CO6: Develop a comprehensive research plan, including a detailed research design, data collection and analysis methods, and a plan for protecting intellectual property

UNIT-I: FUNDAMENTALS OF RESEARCH METHODOLOGY:

Overview of research process and design - Types of Research - Approaches to Research (Qualitative vs Quantitative) - Observation studies, Experiments and Surveys - Use of Secondary and exploratory data to answer the research question - Importance of Reasoning in Research and Research ethics - Documentation Styles (APA/IEEE etc.) - Plagiarism and its consequences

Learning Outcomes

● Recall key concepts of the research process, including different types and approaches to research, and the importance of ethics.

● Differentiate between qualitative and quantitative research approaches and the various uses of secondary data.

● Identify the core principles of research design and ethics, including plagiarism and documentation styles.

● Explain the significance of reasoning and ethical conduct in all stages of the research

process.

● Apply knowledge of different documentation styles, such as APA and IEEE, to properly cite sources and avoid plagiarism

UNIT – II: DATA COLLECTION AND SOURCES

Importance of Data Collection - Types of Data - Data Collection Methods - Data Sources - primary, secondary and Big Data sources - Data Quality & Ethics - Tools and Technology for Data Collection.

Learning Outcomes

● Identify different types of data and the various methods for collecting both primary and secondary data.

● Explain the importance of data quality and ethical considerations in data collection.

● Differentiate between primary, secondary, and Big Data sources.

● Describe the various tools and technologies used for effective data collection.

● Analyze the ethical implications of data collection and ensure data quality in a research study.

UNIT – III: DATA ANALYSIS AND REPORTING

Overview of Multivariate analysis - Experimental research, cause-effect relationship, and development of hypotheses- Measurement systems analysis, error propagation, and validity of experiments - Guidelines for writing abstracts, introductions, methodologies, results, and discussions- Writing Research Papers & proposals.

Learning Outcomes

● Apply knowledge of multivariate analysis and experimental research to develop hypotheses and analyze data.

● Explain the process of measurement systems analysis and error propagation in experimental design.

● Formulate clear and concise abstracts, introductions, and methodologies for research papers.

● Write effective results and discussion sections based on data analysis.

● Develop comprehensive research papers and proposals based on proper data analysis and reporting guidelines

UNIT – IV: UNDERSTANDING INTELLECTUAL PROPERTY RIGHTS

Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

Learning Outcomes

● Recall the fundamental concepts of Intellectual Property (IP) and its evolution.

● Describe the roles of organizations like WIPO and WTO in the establishment of IPR.

● Differentiate between various types of IPR, including trade secrets and trademarks.

● Explain the common rules and features of IPR agreements and the role of UNESCO.

● Analyze the relationship between IPR and biodiversity, and its broader impact

UNIT – V: PATENTS

Patents − objectives and benefits of patent, Concept, features of patent, Inventive step, Specification - Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licenses, Licensing of related patents, patent agents, Registration of patent agents.

Learning Outcomes

● Explain the objectives, benefits, and key features of a patent, including the concept of an inventive step.

● Differentiate between the various types of patent applications and the e-filing process.

● Describe the process of patent examination, grant, and revocation.

● Identify the roles of patent agents and the process for their registration.

● Analyze the concepts of equitable assignments, licenses, and licensing of related patents.

Text Books:

1. Stuart Melville and Wayne Goddard, Research Methodology: An introduction for Science & Engineering students, Juta and Company Ltd, 2004

2. Catherine J. Holland, Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets, Entrepreneur Press, 2007.

Reference Books:

1. Cooper Donald R, Schindler Pamela S and Sharma JK, ―Business Research Methods‖, Tata McGraw Hill Education 11e (2012).

2. Ranjit Kumar , Research Methodology: A Step-by-Step Guide for Beginners. . David Hunt, Long Nguyen, Matthew Rodgers, ―Patent searching: tools & techniques‖, Wiley, 2007.

3. Deborah E. Bouchoux , Intellectual Property: The Law of Trademarks, Copyrights, Patents, and Trade Secrets, 6th Edition, Cengage 2024.

4. Wayne C. Booth, Gregory G. Colomb, Joseph M. Williams, The Craft of Research, 5th Edition, University of Chicago Press, 2024

5. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, ―Professional Programme Intellectual Property Rights, Law and practice‖, September 2013.

6. Peter Elbow, Writing With Power, Oxford University Press, 1998.

Online Resources (Free & Authentic)

● Coursera / edX – Research Methodology and Data Analysis courses

● Springer Link & Science Direct – Latest journals on research design and statistics

● Google Scholar – Free access to research papers

● NCBI Bookshelf – Open-access research methodology resources

● Khan Academy (Statistics & Probability) – For fundamentals of hypothesis testing, regression, and ANOVA.

CO	B.T	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	L1	3	2	-	-	-	-	-	-	1	-	-	-
CO2	L2	3	3	-	2	2	-	1	-	2	-	-	1
CO3	L3	3	3	1	2	3	2	-	2	3	2	3	2
CO4	L4	2	3	1	2	2	2	-	-	3	2	2	3
CO5	L5	2	3	1	1	3	2	-	3	2	2	2	3
CO6	L6	3	3	2	3	3	3	-	3	3	3	3	3

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-I Semester-VLSI Design

Course Code: 25BVL11

RTL SYNTHESIS, SIMULATION AND VERIFICATION
(SKILL COURSE)

L	T	P	C
0	1	2	2

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Demonstrate the process steps required for simulation /synthesis.

CO2: Design and simulate various combinational and sequential circuits using HDL.

CO3: Develop an RTL code for various real time applications.

CO4: Synthesize / Simulate an RTL code for several digital designs

CO5: Build and verify various digital circuits.

Module 1 – Introduction to RTL Design

- RTL design flow: Specification → RTL coding → Synthesis → Simulation → Verification.
- HDL coding styles for synthesis (SystemVerilog/VHDL basics).
- Lab:

1. Write synthesizable Verilog/SystemVerilog code for:
   a) Half Adder, Full Adder
   b) 4-bit Ripple Carry Adder
   c) 4-bit Synchronous Counter (Up/Down)
2. FSM Design: Sequence Detector (e.g., detect "1011").

Module 2 – RTL Synthesis

- Synthesis concepts: mapping RTL to gate-level netlist.
- Constraints: clock, area, power.
- Lab:

1. Synthesize combinational and sequential circuits (Adder, Counter, FSM) using EDA tool
2. Generate gate-level netlist and analyze area, delay, power reports.
3. Apply constraints (clock, timing) and observe impact on synthesis results.

Module 3 – Simulation

- Functional vs. Timing simulation.
- Testbench creation, waveforms, debugging.
- Lab: Run simulations

1. Develop testbenches for:
   a) 4-bit ALU (add, sub, AND, OR).
   b) Universal Shift Register.
2. Perform functional simulation using EDA tools
3. Perform post-synthesis (timing) simulation and compare results with functional simulation.

Module 4 – Verification

- Verification basics: functional verification, assertion-based verification.
- Introduction to UVM/OVM concepts.
- Lab: Writing simple verification testbenches.

1. Write self-checking testbenches for combinational and sequential circuits.
2. Use assertion-based verification (SystemVerilog Assertions – SVA) for protocol checks (e.g., handshaking signals).
3. Coverage-driven verification experiment: Create random test cases for FIFO/Memory

Module 5 – Case Study & Mini Project

- Design, synthesize, and verify a digital subsystem (e.g., ALU, UART, FIFO).
- End-to-end RTL → Synthesis → Simulation → Verification flow.
- Lab: Design, synthesize, simulate, and verify a **digital subsystem** such as:

    1. UART Transmitter/Receiver
    2. Simple CPU Core Module (Instruction Decoder + ALU + Register File)
    3. FIFO Buffer with full/empty flags

Textbooks / References

1. Samir Palnitkar – *Verilog HDL: A Guide to Digital Design and Synthesis.*
2. Michael Ciletti – *Advanced Digital Design with the Verilog HDL.*
3. Chris Spear & Greg Tumbush – *SystemVerilog for Verification.*
4. David Rich – *Design and Verification with SystemVerilog.*

Suggested reading:

1. Samir Palnitkar, "Verilog HDL, a guide to digital design and synthesis", Prentice Hall 2003.
2. Doug Amos, Austin Lesea, Rene Richter, "FPGA based prototyping methodology manual", Xilinx, 2011.
3. Bob Zeidman, "Designing with FPGAs & CPLDs", CMP Books, 2002.

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-I Semester-VLSI Design

Course Code: 25BHS04

ENGLISH FOR RESEARCH PAPER WRITING
(AUDIT COURSE-I)

L	T	P	C
2	0	0	0

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Recall the key language aspects and structural elements of academic writing in research papers.

CO2: Explain the importance of clarity, precision, and objectivity in research writing.

CO3: Apply critical reading strategies and advanced grammar skills to analyze and write research papers.

CO4: Analyze research articles and identify the strengths and limitations of different methodologies.

CO5: Evaluate research papers to check for plagiarism, structure, clarity, and language accuracy.

CO6: Evaluate the effectiveness of different language and technology tools in research writing, including AI-assisted tools and plagiarism detection software.

CO7: Develop a well-structured research paper that effectively communicates complex ideas.

UNIT – I: Fundamentals of Academic English

Academic English - MAP (Message-Audience-Purpose) - Language Proficiency for Writing - Key Language Aspects - Clarity and Precision - Objectivity - Formal Tone - Integrating References - Word order - Sentences and Paragraphs - Link Words for Cohesion - Avoiding Redundancy / Repetition - Breaking up long sentences - Structuring Paragraphs - Paraphrasing Skills – Framing Title and Sub-headings

UNIT – II: Reading Skills for Researchers

Reading Academic Texts - Critical Reading Strategies - Skimming and Scanning - Primary Research Article vs. Review Article - Reading an Abstract - Analyzing Research Articles - Identifying Arguments - Classifying Methodologies - Evaluating Findings - Making Notes

UNIT – III: Grammar Refinement for Research Writing

Advanced Punctuation Usage - Grammar for Clarity - Complex Sentence Structures - Active-Passive Voice - Subject-Verb Agreement - Proper Use of Modifiers - Avoiding Ambiguous Pronoun References - Verb Tense Consistency - Conditional Sentences

UNIT – IV: Mastery in Refining Written Content/Editing Skills

Effective Revisions - Restructuring Paragraph - Editing vs Proofreading, Editing for Clarity and Coherence - Rectifying Sentence Structure Issues - Proofreading for Grammatical Precision – Spellings - Tips for Correspondence with Editors - Critical and Creative Phases of Writing.

UNIT – V: Technology and Language for Research

Digital Literacy and Critical Evaluation of Online Content - Technology and Role of AI in Research Writing – Assistance in Generating Citations and References - Plagiarism and Ethical Considerations – Tools and Awareness – Fair Practices

Textbooks:

1.Bailey. S. Academic Writing: A Handbook for International Students. London and New York: Routledge,2015.

2. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

Reference Books:

1. Craswell, G. Writing for Academic Success, Sage Publications, 2004.

2. Peter Elbow, Writing With Power, E-book, Oxford University Press, 2007

3. Oshima, A. & Hogue, A. Writing Academic English, Addison-Wesley, New York, 2005

4. Swales, J. & C. Feak, Academic Writing for Graduate Students: Essential Skills and Tasks. Michigan University Press, 2012.

5.Goldbort R.Writing for Science, Yale University Press (available on Google Books), 2006

6. Day R.How to Write and Publish a Scientific Paper, Cambridge University Press, 2006

Online Learning Resources:

1. https://nptel.ac.in/noc/courses/noc20/SEM1/noc20-ge04/

2. https://onlinecourses.swayam2.ac.in/ntr24_ed15/preview

3."Writing in the Sciences" – Stanford University (MOOC on Coursera)

https://www.coursera.org/learn/sciwrite

4.Academic Phrasebank – University of Manchester

http://www.phrasebank.manchester.ac.uk

5.OWL (Online Writing Lab) – Purdue University,

https://owl.purdue.edu *(Resources on APA/MLA formats, grammar, structure, paraphrasing)*

6. Zotero or Mendeley (Reference Management Tools) – Useful for managing citations and sources.

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-I Semester-VLSI Design

Course Code: 25BST11

DISASTER MANAGEMENT
(AUDIT COURSE-I)

L	T	P	C
2	0	0	0

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Define and distinguish between hazards and disasters, and explain their types, nature, and impacts.

CO2: Identify and map disaster-prone areas in India and understand the epidemiological consequences of disasters.

CO3: Assess the economic, social, and ecological repercussions of major natural and man-made disasters.

CO4: Demonstrate knowledge of disaster preparedness tools such as remote sensing, meteorological data, risk evaluation, and community awareness.

CO5: Apply risk assessment methods and propose disaster risk reduction strategies at local, national, and global levels.

CO6: Formulate and evaluate structural and non-structural disaster mitigation strategies, with emphasis on Indian programs and emerging trends.

UNIT-I:

Introduction: Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India:

Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics.

UNIT-II:

Repercussions of Disasters and Hazards: Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT-III:

Disaster Preparedness and Management: Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media. Reports: Governmental and Community Preparedness.

UNIT-IV: Risk Assessment:

Disaster Risk -Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT-V:

Disaster Mitigation:

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

Text books:

1. Gupta, H. K. Disaster Management. Universities Press, 2003

2. Singh, R. B. Natural Hazards and Disaster Management. Rawat Publications, 2006.

Reference Books:

1. Coppola, D. P. (2020). Introduction to International Disaster Management (4th ed.). Elsevier.

2. Shaw, R., & Izumi, T. (2022). Science and Technology in Disaster Risk Reduction in Asia. Springer.

3. Wisner, B., Gaillard, J. C., & Kelman, I. (2021). Handbook of Hazards and Disaster Risk Reduction and Management (2nd ed.). Routledge.

4. Saini, V. K. (2021). Disaster Management in India: Policy, Issues and Perspectives. Sage India.

5. Kelman, I. Disaster by Choice: How Our Actions Turn Natural Hazards into Catastrophes, Oxford University Press, 2022

6. Sahni, P. & Dhameja, A. Disaster Mitigation: Experiences and Reflections. Prentice Hall of India, 2004.

Online Resources

- National Disaster Management Authority (NDMA), India: https://ndma.gov.in − official guidelines, reports, and policy frameworks.
- United Nations Office for Disaster Risk Reduction (UNDRR): https://www.undrr.org − Sendai Framework, global risk reduction strategies.
- Global Disaster Alert and Coordination System (GDACS): https://www.gdacs.org − real-time disaster alerts.
- World Health Organization (WHO) − https://www.who.int/emergencies − disaster-related health guidelines.

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-I Semester-VLSI Design

Course Code: 25BHS05

ESSENCE OF INDIAN TRADITIONAL KNOWLEDGE
(AUDIT COURSE-I)

L	T	P	C
2	0	0	0

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Define and explain the concept of traditional knowledge, its nature, characteristics, and scope

CO2: Understand the need for protecting traditional knowledge and its significance in the global economy

CO3: Explain the legal framework and policies related to traditional knowledge protection

CO4: Apply traditional knowledge in different sectors, such as engineering, medicine, agriculture, and biotechnology

CO5: Analyze the importance of traditional knowledge in various contexts, including its historical impact and social change

CO6: Analyze the relationship between traditional knowledge and intellectual property rights, including patents and non-IPR mechanisms

Unit-I: Introduction to traditional knowledge - Definition, Nature and characteristics, scope and importance - Kinds of traditional knowledge - Physical and social contexts in which traditional knowledge develop - Historical impact of social change on traditional knowledge systems - Indigenous Knowledge (IK) – Characteristics - traditional knowledge vis-à-vis indigenous knowledge -Traditional knowledge Vs western knowledge, traditional knowledge vis-à-vis formal knowledge

Learning Outcomes:

At the end of the unit the student will able to:

- Understand the concept of traditional knowledge.
- Contrast and compare characteristics, importance& kinds of traditional knowledge.
- Analyze physical and social contexts of traditional knowledge.
- Evaluate social change on traditional knowledge.

Unit-II: Protection of traditional knowledge- Need for protecting traditional knowledge - Significance of TK Protection - Value of TK in global economy - Role of Government to harness TK.

Learning Outcomes:

At the end of the unit the student will able to:

- Know the need of protecting traditional knowledge.

- Apply significance of TK protection.
- Analyze the value of TK in global economy.
- Evaluate role of government

Unit-III: Legal frame work and TK - A)The Scheduled Tribes and Other Traditional Forest Dwellers (Recognition of Forest Rights) Act, 2006 - Plant Varieties Protection and Farmer's Rights Act, 2001 (PPVFR Act) – B)The Biological Diversity Act 2002 and Rules 2004 - the protection of traditional knowledge bill, 2016 - Geographical Indicators Act 2003.

Learning Outcomes:

At the end of the unit the student will able to:

- Understand legal frame work of TK.
- Contrast and compare the ST and other traditional forest dwellers
- Analyze plant variant protections
- Understand the rights of farmers forest dwellers

Unit-IV: Traditional knowledge and Intellectual property - Systems of traditional knowledge protection - Legal concepts for the protection of traditional knowledge - Certain non-IPR mechanisms of traditional knowledge protection - Patents and traditional knowledge - Strategies to increase protection of traditional knowledge -Global legal FORA for increasing protection of Indian Traditional Knowledge.

Learning Outcomes:

At the end of the unit the student will able to:

- Understand TK and IPR
- Apply systems of TK protection.
- Analyze legal concepts for the protection of TK.
- Evaluate strategies to increase the protection of TK.

Unit-V: Traditional knowledge in different sectors - Traditional knowledge and Engineering - Traditional medicine system - TK and Biotechnology - TK in Agriculture - Traditional societies depend on it for their food and healthcare needs - Importance of conservation and sustainable development of environment - Management of biodiversity, Food security of the country and protection of TK

Learning Outcomes:

At the end of the unit the student will be able to:

- Know TK in different sectors.
- Apply TK in Engineering.
- Analyze TK in various sectors.
- Evaluate food security and protection of TK in the country.

Prescribed Books:

1. Mahadevan, B., Bhat Vinayak Rajat, Nagendra Pavana R.N. *Introduction to Indian Knowledge System: Concepts and Applications*, PHI Learning Pvt.Ltd. Delhi, 2022.

2. Basanta Kumar Mohanta and Vipin Kumar Singh,*Traditional Knowledge System and Technology in India*, PratibhaPrakashan 2012.

Reference Books:

1. Pride of India: A Glimpse into India's Scientific Heritage, Samskrita Bharati, New Delhi.
2. Kak, S.C. "On Astronomy in Ancient India", Indian Journal of History of Science, 22(3), 1987
3. Subbarayappa, B.V. and Sarma, K.V. *Indian Astronomy: A Source Book*, Nehru Centre, Mumbai, 1985.
4. Bag, A.K. *History of Technology in India*, Vol. I, Indian National Science Academy, New Delhi, 1997.
5. Acarya, P.K. *Indian Architecture*, Munshiram Manoharlal Publishers, New Delhi, 1996.
6. Banerjea, P. *Public Administration in Ancient India*, Macmillan, London, 1961.
7. Kapoor Kapil, Singh Avadhesh,*Indian Knowledge Systems Vol – I & II*, Indian Institute of Advanced Study, Shimla, H.P., 2022

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS)

M.Tech-II Semester-VLSI Design

Course Code: 25BVL12

CMOS MIXED SIGNAL IC DESIGN

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Demonstrate first order filter with least interference

CO2: Extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects.

CO3: Design different A/D, D/A, modulators, demodulators and different filter for real time applications.

UNIT-I:

Switched Capacitor Circuits: Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators, first order filters, Switch sharing, biquad filters.

UNIT-II:

Phased Lock Loop (PLL) : Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs- Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT-III:

Data Converter: Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT-IV:

A to D Converters: Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Sigma Delta A/D coverters, Time- interleaved converters.

UNIT-V:

Oversampling Converters: Noise shaping modulators, Decimating filters and interpolating filters,

Higher order modulators, Delta sigma modulators with multi bit quantizers, Delta sigma D/A.

Textbooks:

1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition, 2002

2.CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

3. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edition, 2013

Reference Books:

1.CMOS Integrated Analog-to- Digital and Digital-to-Analog converters- Rudy Van De Plassche, Kluwer Academic Publishers, 2003

2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Inter science, 2005.

3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience,2009

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS)

M.Tech-II Semester-VLSI Design

Course Code: 25BVL13

PHYSICAL DESIGN AUTOMATION

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Understand relation between automation algorithms and constraints posed by VLSI technology.

CO2: Adopt algorithms to meet critical design parameters.

CO3: Design area efficient logics by employing different routing algorithms and shape functions.

CO4: Simulate and synthesis different combinational and sequential logics.

UNIT-I:

VLSI Design Automation Tools: Algorithms and system design, Structural and logic design, Transistor level design, Layout design, Verification methods, Design management tools.

UNIT - II

Layout: Compaction, placement and routing, Design rules, symbolic layout, Applications of compaction. Formulation methods, Algorithms for constrained graph compaction, Circuit representation, Wire length estimation, Placement algorithms, Partitioning algorithms.

UNIT - III

Floor planning and routing: Floor planning concepts, Shape functions and floor planning sizing, Local routing, Area routing, Channel routing, global routing and its algorithms.

UNIT - IV

Simulation and Logic Synthesis: Gate level and switch level modeling and simulation, Introduction to combinationallogic synthesis, ROBDD principles ,implementation, construction and manipulation, Two level logic synthesis.

UNIT - V

High-Level Synthesis: Hardware model for high level synthesis, internal representation of input algorithms, Allocation, assignment and scheduling, scheduling algorithms, Aspects of assignment, High level transformations.

Textbooks:

1. S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley, 1998.

2. N.A. Sherwani, Algorithms for VLSI Physical Design Automation, (3/e), Kluwer, 1999.

Reference Books:

1. S.M. Sait,H.Youssef, VLSI Physical Design Automation, World scientific, 1999.

2. M.Sarrafzadeh, Introduction to VLSI Physical Design, McGraw Hill (IE), 1996

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-II Semester-VLSI Design

Course Code: 25BVL14

SOC TESTING AND VERIFICATION
(PROFESSIONAL ELECTIVE-III)

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Understand the concepts of faults and testing in SoC

CO2: Implement the faults using simulation tools

CO3: Analyze BIST systems

UNIT-I:

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT - II

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT - III

Testability Measures: SCOAP Controllability and observablity ,High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT - IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-
Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT - V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Textbooks:

1. M.L. Bushnell, V. D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits”, Kluwer Academic Pulishers.

2. M. Abramovici, M.A.Breuer and A.D Friedman, “Digital Systems and Testable Design”, Jaico Publishing House.

Reference Books:

1. P.K. Lala, “Digital Circuits Testing and Testability”, Academic Press.

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS)

M.Tech-II Semester-VLSI Design

Course Code: 25BVL15

SEMICONDUCTOR MEMORY DESIGN AND TESTING (PROFESSIONAL ELECTIVE-III)

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Get complete knowledge regarding different types of memories, their architectural and different packing techniques of memories.

CO2: Build fault models for memory testing.

CO3: Analyze different parameters that lead malfunctioning of memories.

CO4: Design reliable memories with efficient architecture to improve processes times and power.

UNIT-I:

Random Access Memory Technologies :SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT – II:

Non-volatile Memories: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT – III:

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance : RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non- volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT – IV:

Semiconductor Memory Reliability and Radiation Effects: General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test
structures.

UNIT – V:

Advanced Memory Technologies and High-density Memory Packing Technologies

Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

Textbooks:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma, 2002, Wiley.

Reference Books:

1. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, First Edition. Prentice all.

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SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-II Semester-VLSI Design

Course Code: 25BVL16

ADVANCED VLSI INTERCONNECTS
(PROFESSIONAL ELECTIVE-III)

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Understand the transmission line parameters of VLSI interconnect.

CO2: Learn the novel and emerging solutions for future VLSI interconnect technologies.

CO3: Analyze the impact of inductive effects in high-speed interconnects.

CO4: Examine the influence of quantum effects in nanoscale interconnects.

UNIT – I:

Introduction: Introduction to VLSI Interconnects, The Distributed RC Interconnect Model, Elmore Delay in Interconnects, Scaling Effects in Interconnects, Simulation and Delay Mitigation in RC Interconnects.

UNIT – II:

Inductive Effects: Inductive Effects in Interconnects, Distributed RLC Interconnect Model, Transmission Line Equations, When to Consider the Inductive Effects?, Equivalent Elmore Model for RLC Interconnects, Two-Pole Model of RLC Interconnects from ABCD Parameters, RLC Interconnect Simulation.

UNIT – III:

Resistance at High Frequencies, Power Dissipation due to Interconnects, Electro migration in Interconnects, Mitigation of Electro migration**.**

UNIT – IV:

Crosstalk: Capacitive Coupling in Interconnects, Crosstalk Effects in Two Identical Interconnects, Mitigation Techniques, Analysis and Simulation of Coupled Interconnects. Extraction of Capacitance, Extraction of Inductance, Estimation of Interconnect Parameters from S-parameters.

UNIT – V:

Quantum Effects: Quantum Conductance, Quantum Capacitance, Kinetic Inductance, Graphene Nanoribbon Interconnects, Analysis and Simulation of Interconnect Considering Quantum Effects.

Textbooks:

1. Ashok K. Goel, High-Speed VLSI Interconnects.
2. Y.S.Diamand, Advanced Nanoscale ULSI Interconnects: Fundamental sand Applications, Engineering.

Reference Books:

1. H.S Philip Wong and DejiAkinwande, Carbon nanotube and Graphene Device Physics, 2011.OtherSuggestedReadings:NPTELCourses (https://onlinecourses.nptel.ac.in/noc22_ee125/preview)

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-II Semester-VLSI Design

Course Code: 25BVL17

LOW POWER VLSI DESIGN
(PROFESSIONAL ELECTIVE-IV)

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect

CO2: Implement Low power design approaches for system level and circuit level measures.

CO3: Design low power adders, multipliers and memories for efficient design of systems.

UNIT – I:

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Static and Dynamic Power Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT – II:

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT – III:

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques – Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT – IV:

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT – V:

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

Textbooks:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional

Engineering.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Low Power CMOS Design – Anantha Chandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-II Semester-VLSI Design

Course Code: 25BVL18

ALGORITHMS FOR VLSI DESIGN
(PROFESSIONAL ELECTIVE-IV)

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Understand the VLSI design methodologies

CO2: Understand the optimization methods.

CO3: Learn various methodologies in floor planning.

CO4: Explore the tools used in Physical Design Automation

UNIT – I:

PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT – II:

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT – III:

LAYOUT COMPACTION, PLACEMENT, FLOOR PLANNING AND ROUTING: Problems, Concepts and Algorithms**.**

MODELLING AND SIMULATION:

Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT – IV:

LOGIC SYNTHESIS AND VERIFICATION:

Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

HIGH-LEVEL SYNTHESIS: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT – V:

PHYSICAL DESIGN AUTOMATION OF FPGAs

FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.

PHYSICAL DESIGN AUTOMATION OF MCMs

MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCMs

Textbooks:

1. Algorithms for VLSI Design Automation, S.H.Gerez, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd.1999.

2. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed., Springer International Edition, 2005.

Reference Books:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill &Peterson, Wiley, 1993.

2. Modern VLSI Design: Systems on silicon – Wayne Wolf, 2nd Ed., Pearson Education Asia, 1998

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-II Semester-VLSI Design

Course Code: 25BVL19

VLSI SIGNAL PROCESSING
(PROFESSIONAL ELECTIVE-IV)

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Study the existing architectures suitable for VLSI.

CO2: Understand the concepts of folding and unfolding algorithms and applications.

CO3: Design new architectures suitable for VLSI.

CO4: Implement fast convolution algorithms

UNIT – I:

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT – II:

Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multi rate systems Unfolding-Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding.

UNIT – III:

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT – IV:

Fast Convolution: Introduction – Cook - Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT – V:

Low Power Design: Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipe lines, Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches

Textbooks:

1. Keshab K. Parthi, VLSI Digital Signal Processing- System Design and Implementation, Wiley Inter Science, 1998.
2. Kung S. Y, H. J. While House, T. Kailath ,VLSI and Modern Signal processing , Prentice Hall, 1985.

Reference Books

1. Jose E. France, Yannis Tsividis, Design of Analog – Digital VLSI Circuits Telecommunications and Signal Processing , Prentice Hall, 1994.
2. Medisetti V. K ,VLSI Digital Signal Processing , IEEE Press (NY), 1995

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS)

M.Tech-II Semester-VLSI Design

Course Code: 25BVL20

CMOS MIXED SIGNAL IC DESIGN LAB

L	T	P	C
0	0	4	2

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Design and simulate op-amp for given specifications

CO2: Design and simulate data converter for given specifications

CO3: Design and simulate PLL and VCO for given specifications

CO4: Understand the Significance of Pre-Layout Simulation and Post-Layout Simulation.

List of Experiments:

The students are required to design and implement the Circuit and Layout of the following Experiments using CMOS 130nm Technology.

Cycle 1:

1) Fully compensated op-amp with resistor and miller compensation
2) High speed comparator design
   a. Two stage cross coupled clamped comparator
   b. Strobed Flip-flop
3) Data converter

Cycle 2:

1) Switched capacitor circuits
   a. Parasitic sensitive integrator
   b. Parasitic insensitive integrator
2) Design of PLL
3) Design of VCO
4) Band gap reference circuit
5) Layouts of All the circuits Designed and Simulated

Software:

Mentor Graphics/ Cadence/ Tanner/Industry Equivalent Standard Software Tools

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

References:

1. David A johns, Ken Martin, Analog Integrated Circuit Design, Wiley, 2008.
2. R. Gregorian and G.C Ternes, Analog MOS Integrated Circuits for Signal Processing, Wiley,1986.
3. Roubik Gregorian, Introduction to CMOS OpAmp and Comparators, Wiley, 1999.
4. Alan Hastlings, The art of Analog Layout, Wiley, 2005.

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS)

M.Tech-II Semester-VLSI Design

Course Code: 25BVL21

PHYSICAL DESIGN AUTOMATION LAB

L	T	P	C
0	0	4	2

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Learn the implementation of different Physical Design Automation algorithms

CO2: Implement different graph algorithms

CO3: Implement different partitioning algorithms

CO4: Implement different floor planning algorithms

CO5: Implement different routing algorithms

List of Experiments:

Cycle 1:

1) Graph algorithms
   a) Graph search algorithms
      i. Depth first search
      ii. Breadth first search
   b) Spanning tree algorithm
      i. Kruskal‟s algorithm
   c) Shortest path algorithm
      i. Dijkstra algorithm
      ii. Floyd- Warshall algorithm
   d) Steiner tree algorithm
2) Computational geometry algorithm
   a) Line sweep method
   b) Extended line sweep method

Cycle 2:

3) Partitioning algorithms
   a) Group migration algorithms
      I. Kernighan –Lin algorithm
      II. Extensions of Kernighan-Lin algorithm

i) Fiduccias –Mattheyses algorithm

ii) Goldberg and Burstein algorithm

b) Simulated annealing and evolution algorithms

i. Simulated annealing algorithm

ii. Simulated evolution algorithm

III) Metric allocation method

4) Floor planning algorithms

i) Constraint based methods

ii) Integer programming based methods

iii) Rectangular dualization based methods

iv) Hierarchical tree based methods

v) Simulated evolution algorithms

vi) Time driven Floor planning algorithms

5) Routing algorithms

I) Two terminal algorithms

a) Maze routing algorithms

i) Lee‟s algorithm

ii) Soukup‟s algorithm

iii) Hadlock algorithm

b) Line-Probe algorithm

c) Shortest path based algorithm

II) Multi terminal algorithm

a) Stenier tree based algorithm

i) SMST algorithm

ii) Z-RST algorithm

Software required: C/C++ Programming Language /Relevant software

Text Books:

1) Naveed Shervani, Algorithms for Physical Design Automation, 3rd Edition, Kluwer Academic,1998.
2) Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press,200

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS)

M.Tech-II Semester-VLSI Design

Course Code: 25BCS22

QUANTUM TECHNOLOGIES AND APPLICATIONS (MANDATARY COURSE)

L	T	P	C
2	0	0	2

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Explain fundamental quantum concepts conceptually

CO2: Distinguish classical information systems from quantum information frameworks

CO3: Identify the principal theoretical limitations in building quantum computers

CO4: Describe the conceptual basis of quantum communication and computation

CO5: Discuss current applications, technological trajectories, and career opportunities in the quantum domain

Unit 1: Foundations of Quantum Theory and Technologies

Transition from classical to quantum physics. Key conceptual principles: Superposition, Entanglement, Uncertainty, Wave-particle duality. Quantum states and measurement; the role of the observer. Representative quantum systems: electrons, photons, atoms. Concept of quantization and discrete energy levels. Strategic relevance of quantum technologies. Overview of major domains: Computing, Communication, Sensing. Global quantum initiatives: India's National Quantum Mission, EU Quantum Flagship, USA, China.

Unit 2: Conceptual Structure of Quantum Information

Qubits: qualitative understanding using spin and polarization. Classical bits vs quantum bits: distinctions and implications. Quantum systems (non-engineering perspective): trapped ions, superconducting qubits, photonics. Coherence and decoherence mechanisms. Abstract notions: quantum states, measurement operators, Hilbert space—interpretation without mathematics. Entanglement and non-locality as foundational resources. Quantum vs classical information principles; philosophical considerations.

Unit 3: Building a Quantum Computer – Challenges and Requirements

Conceptual prerequisites for functional quantum hardware. Fragility of quantum states: decoherence, noise, stability issues. Requirements: isolation, error resilience, scalability, control. Why maintaining entanglement is difficult; theoretical necessity of quantum error correction. Comparative overview of hardware platforms (superconducting circuits, trapped

ions, photonics).Current progress vs scientific constraints; conceptual view of quantum software's role.

Unit 4: Quantum Communication and Computing

(Redundant explanations removed, retaining only unique themes.)Quantum vs classical communication paradigms. Essentials of Quantum Key Distribution (QKD) and its security rationale. Entanglement enabled communication protocols. Concept of the Quantum Internet and secure global networking. Introduction to quantum computing and quantum parallelism. Conceptual comparison of classical and quantum gate operations. Challenges: decoherence, noise, and the necessity of error correction frameworks.

Unit 5: Applications, Industry, and Future Directions

Application domains: Healthcare and drug discovery, Material science and chemistry, Optimization and logistics, Quantum sensing and precision timing. Case studies: IBM, Google, Microsoft, PsiQuantum. Ethical, societal, and policy considerations. Barriers to adoption: cost, skilled workforce, standards. Emerging research and career landscapes; India's strategic opportunity in the global quantum ecosystem.

Textbooks

1. Nielsen & Chuang, Quantum Computation and Quantum Information, Cambridge University Press, 2010.
2. Rieffel & Polak, Quantum Computing: A Gentle Introduction, MIT Press, 2011. 3. Chris Bernhardt, Quantum Computing for Everyone, MIT Press, 2019.

Reference Books

1. David McMahon, Quantum Computing Explained, Wiley, 2008.
2. Kaye, Laflamme, Mosca, An Introduction to Quantum Computing, OUP, 2007.
3. Scott Aaronson, Quantum Computing Since Democritus, CUP, 2013.
4. Susskind & Friedman, Quantum Mechanics: The Theoretical Minimum, Basic Books, 2014.
5. Rosenblum & Kuttner, Quantum Enigma, OUP, 2011.
6. Benenti et al., Principles of Quantum Computation and Information, World Scientific, 2004.
7. DST India and MeitY: Official Quantum Mission Reports, 2020 onwards.
8. Quantum Flagship EU: Roadmaps and Strategy Documents.

Online Learning Resources

1. IBM Quantum Experience & Qiskit Textbook Coursera – Quantum Mechanics and Quantum
2.Computation (UC Berkeley) edX – Quantum Internet & Quantum Computers
3.YouTube – Quantum Computing for the Determined (Michael Nielsen)

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-II Semester-VLSI Design

Course Code: 25BVL22

COMPREHENSIVE VIVA VOCE

L	T	P	C
0	0	0	2

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-II Semester-VLSI Design

Course Code: 25BMB02

PEDAGOGY STUDIES
(AUDIT COURSE-II)

L	T	P	C
2	0	0	0

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Define and explain key concepts, frameworks, and methodologies in pedagogy and teacher education research.

CO2: Critically analyze pedagogical practices used in diverse classroom settings, with reference to teacher education and curriculum design.

CO3: Evaluate the effectiveness of pedagogical approaches using quality assessment tools and theory of change models.

CO4: Apply evidence-based strategies to improve classroom practices, curriculum alignment, and teacher professional development.

CO5: Identify and address barriers to learning through innovative pedagogical strategies

CO6: Design and propose research studies that contribute to filling gaps in pedagogy, curriculum, and teacher education, with focus on dissemination and impact.

UNIT – I: Foundations of Pedagogy

Introduction to pedagogy and its importance in education - Historical and philosophical foundations of pedagogy - Theories of learning and teaching (behaviorist, cognitive, constructivist) - Role of pedagogy in shaping educational practices - Role of technology in modern pedagogy (ICT, e-learning, blended learning

UNIT - II Teaching-Learning Processes

Understanding the teaching-learning process - Lesson planning and curriculum design - Strategies for effective teaching and learning (expository, collaborative, experiential) - Use of technology to enhance teaching-learning processes (multimedia, simulations, gamification)

UNIT - III Technology Integration in Education

Educational technology and system design - Instructional design models (ADDIE, ASSURE, Dick and Carey Model) - Emerging trends in e-learning (social learning, MOOCs, mobile learning) - ICT tools for teaching and learning (Learning Management Systems, online resources).

UNIT - IV Pedagogy and Assessment

Pedagogy, pedagogical analysis, and assessment - Types of assessment (placement, formative, diagnostic, summative) - Technology-based assessment tools (online quizzes, polls, discussions) - Rubrics for self and peer evaluation- Reflective Practices.

UNIT - V Contemporary Issues and Trends

Inclusive education and technology (assistive technology, accessibility) - Change management and innovation in education - Quality assurance and evaluation in education (TQM, Six Sigma) - Future trends in pedagogy and technology (AI, AR, VR in education) - Personalized learning and adaptive teaching.

Textbooks:

1. Alexander, R. J. Essays on Pedagogy. Routledge, 2008.
2. Shulman, L. S. The Wisdom of Practice: Essays on Teaching, Learning, and Learning to Teach. Jossey-Bass, 2004

Reference Books:

1. Teaching for the Future: Effective Teacher Education and Pedagogical Practices. OECD Publishing., 2021
2. Fullan, M., & Edwards, M. System Change in Education: Sustainability and Impact. Routledge, 2022.
3. Coe, R., Rauch, C., Kime, S., & Singleton, D. Great Teaching Toolkit: Evidence Review. Evidence Based Education., 2020
4. Zeichner, K. M. The Struggle for the Soul of Teacher Education. Routledge, 2024
5. UNESCO. Global Education Monitoring Report: Pedagogy, Teachers and Learning. UNESCO Publishing, 2024
6. Hattie, J. Visible Learning: A Synthesis of Over 800 Meta-Analyses Relating to Achievement. Routledge., 2009
7. Darling-Hammond, L. Teacher Education Around the World: What Can We Learn from International Practice? Routledge, 2007

Online Resources

- UNESCO Education Resources – https://www.unesco.org/education
- OECD Education and Skills – https://www.oecd.org/education
- ERIC (Education Resources Information Center) – https://eric.ed.gov (peer-reviewed papers, reports).
- World Bank Education – https://www.worldbank.org/en/topic/education (research reports on teacher development in developing countries).
- NPTEL/SWAYAM MOOCs – Teacher education and pedagogy-focused courses.

- Google Scholar Alerts – set alerts for "pedagogical practices", "teacher education", "curriculum research" for the latest academic papers.

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-II Semester-VLSI Design

Course Code: 25BHS06

YOGA FOR STRESS MANAGEMENT
(AUDIT COURSE-II)

L	T	P	C
2	0	0	0

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Explain the eight limbs of Yoga (Ashtanga) and their interrelationship in holistic development.

CO2: Demonstrate understanding of Yama and Niyama as ethical guidelines and apply them in personal and professional life

CO3: Differentiate between do's and don'ts in daily life with reference to Yogic principles like ahimsa, satya, and swadhyaya..

CO4: Perform selected asanas and pranayama techniques with correct posture, breathing, and awareness.

CO5: Evaluate the physical, mental, and emotional benefits of yoga practices in stress reduction, concentration, and self-discipline.

CO6: Integrate yoga philosophy and practices into a personal routine for sustainable health and inner growth.

UNIT – I:

Definitions of Eight parts of yoga.(Ashtanga)

UNIT - II

Yam and Niyam.

UNIT - III

Do's and Don'tsin life.

i) Ahinsa, satya, astheya, bramhacharya and aparigraha

ii) Shaucha, santosh, tapa, swadhyay, ishwar pranidhan

UNIT - IV

Asanand Pranayam.

UNIT - V

i) Various yoga poses and their benefits for mind and body

ii) Regularization of breathing techniques and its effects-Types of pranayam

Textbooks:

1. Alexander, R. J. Essays on Pedagogy. Routledge, 2008.
2. Shulman, L. S. The Wisdom of Practice: Essays on Teaching, Learning, and Learning to Teach. Jossey-Bass, 2004

Textbooks

1. Swami Prabhavananda and Christopher Isherwood (translation & commentary), Patanjali Yoga Sutras,Sri Ramakrishna Math, 1953.

2. B.K.S. Iyengar, Light on Yoga, Thorsons, 2003.

Reference Books

1. T.K.V. Desikachar, The Heart of Yoga: Developing a Personal Practice, Inner Traditions 2nd Edition, 1999.

2. Acharya Yatendra, Yoga & Stress Management, Fingerprint Publishers, 2019

3. Yamini Muthanna, The Power of Yoga, Om Books International, 2015.

4. Nayaswami Devarshi, Kriya Yoga: Spiritual Awakening for the New Age, Ananda Sangha Publications, 2023.

Online Resources

- NPTEL / SWAYAM Online Courses – Yoga and Physical Education modules.
- AYUSH Ministry Website: https://yoga.ayush.gov.in – official yoga resources, protocols, and research.
- Yoga Journal: https://www.yogajournal.com – practical guides, research updates, asana tutorials.
- Art of Living Foundation: https://www.artofliving.org – pranayama, meditation, and wellness practices.
- YouTube Channels (scholarly & practice-based): o Sivananda Yoga Vedanta Centre o Yoga with Adriene (for practical asana guidance)

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS)

M.Tech-II Semester-VLSI Design

Course Code: 25BHS07

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS (AUDIT COURSE-II)

L	T	P	C
2	0	0	0

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Define and explain key concepts of self-awareness, personality, and personal growth.

CO2: Identify and apply strategies of emotional intelligence to regulate emotions and build effective interpersonal relationships.

CO3: Demonstrate positive thinking, gratitude, and resilience to overcome personal and professional challenges.

CO4: Analyze barriers to effective communication and apply verbal and non-verbal communication techniques in diverse contexts

CO5: Prepare, deliver, and evaluate effective presentations and public speeches with confidence.

CO6: Develop leadership and teamwork skills to collaborate, negotiate, and solve problems in group settings.

UNIT – I: Self-Awareness and Personal Growth

Understanding personality and its development- Identifying strengths, weaknesses, opportunities, and challenges (SWOC analysis)- Setting personal and professional goals- Practicing Self-Reflection and Journaling (Activities: Personalitya assessments, self reflection exercises, group discussions, SWOC analysis worksheet, Action Plan, SMART goal activities, Reflective journaling, Self-care Planning).

UNIT – II: Emotional Intelligence and Interpersonal Skills

Understanding emotional intelligence and its importance - Developing self-awareness, self-regulation, and motivation - Building effective communication and interpersonal skills - Conflict resolution and negotiation strategies. (Activities: Emotional Intelligence Quiz, Self-Reflection exercises, feedback sessions, mindfulness exercises, Positive self-talk, Active Listening exercises, conflict-resolution Role-play, Case studies & Group activities).

UNIT – III: Positive Thinking and Attitude

Understanding the power of positive thinking- Developing a growth mindset and resilience - Practicing gratitude and mindfulness- Overcoming negative thoughts and behaviors (Activities on positive thinking, growth mindset, mindfulness and self-care plan for overcoming negative thoughts)

UNIT – IV: Effective Communication and Presentation Skills

Understanding the importance of effective communication- Developing verbal and non-verbal communication skills- Preparing and delivering effective presentations- Building confidence and public speaking skills (Activities: Group discussions, Case studies, Role-Play, Non-verbal communication exercises, Practice presentations, Peer feedback, Public speaking exercises, Storytelling, Debates).

UNIT – V: Leadership and Teamwork

Understanding leadership styles and qualities - Developing leadership skills and qualities- Building effective teams and teamwork strategies- Practicing collaboration and problem-solving

(Activities: Case studies, Group discussions, Debates, Leadership role-playing, team building activities, Group projects, Collaborative problem-solving exercies, feedback sessions)

Prescribed Books

1. Daniel Goleman,Emotional Intelligence: Why It Can Matter More Than IQ, Bantam Books, 2017.

2. Stephen R. Covey, The 7 Habits of Highly Effective People, Simon & Schuster, 2020.

Reference Books

1. Dale Carnegie, How to Win Friends and Influence People, Simon & Schuster, 2020.

2. Brian Tracy, Goals!: How to Get Everything You Want Faster Than You Ever Thought Possible, Berrett-Koehler Publishers, 2021.

3. Robin Sharma, The 5 AM Club: Own Your Morning, Elevate Your Life, HarperCollins, 2020.

4. Carol S. Dweck, Mindset: The New Psychology of Success, Random House, 2016.

5. Daniel H. Pink,Drive: The Surprising Truth About What Motivates Us, Riverhead Books, 2018.

6. John C. Maxwell, Leadershift: 11 Essential Changes Every Leader Must Embrace, HarperCollins, 2019.

Online Resources

1. Coursera – Personal Development Specialization (https://www.coursera.org)
2. edX – Leadership and Emotional Intelligence Courses (https://www.edx.org)
3. FutureLearn – Mindfulness and Resilience Training (https://www.futurelearn.com)
4. MindTools – Practical resources on leadership, communication, and emotional intelligence (https://www.mindtools.com)
5. Positive Psychology – Articles and tools on resilience, gratitude, and well-being (https://positivepsychology.com)
6. TED Talks – Inspirational talks on leadership, communication, and self-growth (https://www.ted.com)
7. Harvard Business Review (HBR) – Leadership, negotiation, and workplace communication (https://hbr.org)

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS)

M.Tech-III Semester-VLSI Design

Course Code: 25BVL23

BICMOS TECHNOLOGY AND APPLICATIONS (PROFESSIONAL ELECTIVE-V)

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Demonstrate in-depth knowledge in Bi-CMOS Technology.

CO2: Analyze complex engineering problems critically for conducting research in Bi-CMOS Technology.

CO3: Solve engineering problems with wide range of solutions in Radio Frequency Integrated circuits.

CO4: Realize different digital circuits using Bi-CMOS Technology

UNIT - I

BiCMOS Process Technology: CMOS Process Technology, Bipolar Process Technology, Isolation in CMOS and Bipolar Technologies, BiCMOS Technology, BiCMOS Design Rules.

UNIT - II

Device Design Considerations: Design Considerations for MOSFET's, Design Considerations for Bipolar Transistors, BiCMOS Device Design Considerations.

BiCMOS Device Scaling: MOS Device Scaling, Bipolar Device Scaling.

UNIT - III

Device Modeling: Modeling of the MOS Transistor: MOSFET Structure and Operation, SPICE Models of the MOS Transistor, Analytical Model for Short-Channel MOS Devices.

Modeling of the Bipolar Transistor: BJT Structure and Operation, Ebers-Moll Model, Bipolar Models in SPICE.

UNIT - IV

BiCMOS Digital Integrated Circuits: BiMOS Totem-Pole Inveter: DC Characteristics, Transient Analysis, Delay Dependence on the Device Parameters, BiCMOS Circuit Design, Comparing CMOS and BiCMOS Inverters Speed, BiCMOS Gates.

UNIT - V

BiCMOS Digital Circuit Applications: Adders, Multiplier, Random Access Memory,

Programmable Logic Arrays, BiCMOS Logic Cells, BiCMOS Gate Arrays.

Textbooks:

1. Sherif H.K. Embabi, Abdellatif Bellaouar& Mohamed I. Elmasry "Digital BiCMOS Integrated Circuit Design" Springer Science+ BusÎness Media, LLC.
2. A L ALVAREZ, BICMOS Technology & Applications, Kluwer Academic Publishers.

Reference Books:

1. Kiat-Seng yeo, Samir S. Rofail, Wang-Ling Goh, CMOS/BiCMOS ULSI, Pearson Education.
2. James C. Daly, Denis P. Galipeau, Analog BiCMOS Design: Practices & Pitfalls, CRC Press
3. KlaasJan de Langen, Johan Huijsing, Compact Low-Voltage and High-Speed CMOS, BiCMOS and Bipolar Operational Amplifiers, Springer Science

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS)

M.Tech-III Semester-VLSI Design

Course Code: 25BVL24

OPTIMIZATION TECHNIQUES AND APPLICATIONS IN VLSI DESIGN (PROFESSIONAL ELECTIVE-V)

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Understand basics of statistical modeling

CO2: Analyze performance of CMOS circuits with respect to power, area and speed

CO3: Acquire complete knowledge regarding the various algorithms used for optimization of power and area.

UNIT - I

Statistical Modeling: Modeling sources of variations, Monte Carlo techniques, Process variation modeling-Pelgrom's model, Principle component based modeling, Quad tree based modeling, Performance modeling- Response surface methodology, delay modeling, interconnect delay models.

UNIT - II

Statistical Performance, Power and Yield Analysis: Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT - III

Convex Optimization: Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting-Monomial fitting, Max monomial fitting, Polynomial fitting.

UNIT - IV

Genetic Algorithm: Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, mapping for FPGA-Automatic test generation-Partitioning algorithm Taxonomy- Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement GASP algorithm-unified algorithm.

UNIT - V

GA Routing Procedures and Power Estimation: Global routing-FPGA technology mapping- circuit generation-test generation in a GA frame work-test generation procedures, Power estimation- application of GA Standard cell placement – GA for ATG-problem encoding-fitness function-GA Vs Conventional algorithm.

Textbooks:

1. Statistical Analysis and Optimization for VLSI: Timing and Power –Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation –Pinaki Mazumder, E. Mrudnick, Prentice Hall,1998.

Reference Books:

1. Convex Optimization- Stephen Boyd, LievenVandenberghe, Cambridge University Press,2004

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-III Semester-VLSI Design

Course Code: 25BVL25

SoC ARCHITECTURE
(PROFESSIONAL ELECTIVE-V)

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Understand the basics related to SoC architecture and different approaches related to SoC Design.

CO2: Select an appropriated robust processor for SoC Design

CO3: Select an appropriate memory for SoC Design.

CO4: Realize real time case studies

UNIT - I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory &Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT - II

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Microarchitecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instruction extensions, VLIW Processors, Superscalar Processors

UNIT - III

Memory Design for SOC: Overview: SOC external memory, SOC Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Other Types of Cache, Split – I, and D – Caches, Multilevel Caches, SOC Memory System, Models of Simple Processor – memory interaction.

UNIT - IV

Interconnect, Customization and Configurability: Interconnect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

SOC Customization: An overview, Customizing Instruction Processor, Reconfigurable Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT - V

Application Studies / Case Studies: SOC Design approach; AES-algorithms, Design and evaluation; Image compression–JPEG compression.

Textbooks:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber, 2ndEdition, 2000, Addison Wesley Professional.

Reference Books:

1.Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer

2.Co-Verification of Hardware and Software for ARM Systemon Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.

3.System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-III Semester-VLSI Design

Course Code: 25BCM26

IoT AND ITS APPLICATIONS
(OPEN ELECTIVE-I)

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Apply the Knowledge in IOT Technologies and Data management.

CO2: Determine the values chains Perspective of M2M to IOT.

CO3: Implement the state of the Architecture of an IOT.

CO4: Compare IOT Applications in Industrial & real world.

CO5: Demonstrate knowledge and understand the security and ethical issues of an IoT.

UNIT I:

Fundamentals of IoT: Evolution of Internet of Things, Enabling Technologies, IoT Architectures, oneM2M, IoT World Forum (IoTWF) and Alternative IoT models, Simplified IoT Architecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of an IoT ecosystem, Sensors, Actuators, Smart Objects and Connecting Smart Objects. IoT Platform overview: Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards..

UNIT II:

IoT Protocols: IT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: CoAP and MQTT.

UNIT III: :

Design and Development: Design Methodology, Embedded computing logic, Microcontroller, System on Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming.

UNIT IV:

Data Analytics and Supporting Services: Structured Vs Unstructured Data and Data in Motion Vs Data in Rest, Role of Machine Learning – No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, Xively Cloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management with NETCONF-YANG.

UNIT V:

Case Studies/Industrial Applications: IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino).

Text Books:

1. IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, Cisco Press, 2017.
2. Internet of Things – A hands-on approach, Arshdeep Bahga, Vijay Madisetti, Universities Press,2015

Reference Books:

1. The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012 (for Unit 2).
2. From Machine-to-Machine to the Internet of Things – Introduction to a New Age of Intelligence‖, Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand. David Boyle and Elsevier, 2014.
3. Architecting the Internet of Things, Dieter Uckelmann, Mark Harrison, Michahelles and Florian (Eds), Springer, 2011.

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-III Semester-VLSI Design

Course Code: 25BCS01

ADVANCED DATA STRUCTURES AND ALGORITHMS
(OPEN ELECTIVE-I)

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Implement and manipulate linear data structures like singly/doubly linked lists, circular lists, stacks, and queues using dynamic memory allocation.

CO2: Apply and analyze searching and sorting algorithms including linear, binary search, bubble, selection, insertion, quick, and merge sort.

CO3: Design and implement dictionaries and hashing techniques to efficiently store and retrieve data.

CO4: Construct and operate on trees and priority queues, performing insertion, deletion, and traversal operations

CO5: Compare and implement balanced search trees (AVL, Red-Black, Splay, B-Trees) for optimized data access and storage.

UNIT I: Introduction

Introduction to Data Structures, Singly Linked Lists, Doubly Linked Lists, Circular Lists-Algorithms. Stacks and Queues: Algorithm Implementation using Linked Lists.

UNIT II: Searching and Sorting

Linear and Binary Search Methods, Sorting: -Basic sorting techniques, Radix Sort, Bucket Sort, Shell Sort Trees- Binary trees, Properties, Representation and Traversals, Expression Trees (Infix, prefix, postfix). Graphs-Basic Concepts, Storage structures and Traversals.

UNIT III: :Dictionaries and Hashing

Dictionaries: Definition, Dictionary Abstract Data Type, Implementation of Dictionaries.

Hashing: Review of Hashing, Hash Function, Collision Resolution Techniques in Hashing, Separate Chaining, Open Addressing, Linear Probing, Quadratic Probing, Double Hashing, Rehashing, Extendible Hashing

UNIT IV: Priority queues

Definition, ADT, Realizing a Priority Queue Using Heaps, Definition, Insertion, Deletion .Search Trees- Binary Search Trees, Definition, ADT, Implementation, Operations- Searching, Insertion, Deletion.

UNIT V: Search Trees

AVL Trees, Definition, Height of AVL Tree, Operations-, Insertion, Deletion and Searching, Introduction to Red-Black and Splay Trees, B-Trees, Height of B-Tree, Insertion, Deletion and Searching, Comparison of Search Trees.

Text Books:

1. Data Structures: A Pseudo Code Approach, 2/e, Richard F.Gilberg, Behrouz A. Forouzon and Cengage

2. Data Structures, Algorithms and Applications in java, 2/e, SartajSahni, University Press

Reference Books:

1. Data Structures and Algorithm Analysis, 2/e, Mark Allen Weiss, Pearson.

2. Data Structures and Algorithms, 3/e, Adam Drozdek, Cengage

3. C and Data Structures: A Snap Shot Oriented Treatise Using Live Engineering Examples, N.B.Venkateswarulu, E.V.Prasad and S Chand & Co.

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-III Semester-VLSI Design

Course Code: 25BCS04

ENTERPRISE CLOUD CONCEPTS
(OPEN ELECTIVE-I)

L	T	P	C
3	0	0	3

Course Outcomes:

After successful completion of the course, the student will be able to:

CO1: Understand importance of cloud architecture.

CO2: Illustrating the fundamental concepts of cloud security.

CO3: Analyze various cloud computing mechanisms.

CO4: Understanding the architecture and working of cloud computing

Unit - I

Understanding Cloud Computing: Origins and influences, Basic Concepts and Terminology, Goals and Benefits, Risks and Challenges. Fundamental Concepts and Models: Roles and Boundaries, Cloud Characteristics, Cloud Delivery Models, Cloud Deployment Models.

Unit - II

Cloud-Enabling Technology: Broadband Networks and Internet Architecture, Data Center Technology, Virtualization Technology CLOUD COMPUTING MECHANISMS: Cloud Infrastructure Mechanisms: Logical Network Perimeter, Virtual Server, Cloud Storage Device, Cloud Usage Monitor, Resource Replication

Unit - III

Cloud Management Mechanisms: Remote Administration System, Resource Management System, SLA Management System, Billing Management System, Case Study Example Cloud Computing Architecture

Fundamental Cloud Architectures: Workload Distribution Architecture, Resource Pooling Architecture, Dynamic Scalability Architecture, Elastic Resource Capacity Architecture, Service Load Balancing Architecture, Cloud Bursting Architecture, Elastic Disk Provisioning Architecture, Redundant Storage Architecture, Case Study Example

Unit - IV

Cloud-Enabled Smart Enterprises Introduction, Revisiting the Enterprise Journey, Service-

Oriented Enterprises, Cloud Enterprises, Smart Enterprises, The Enabling Mechanisms of Smart Enterprises Cloud-Inspired Enterprise Transformations Introduction, The Cloud Scheme for Enterprise Success, Elucidating the Evolving Cloud Idea, Implications of the Cloud on Enterprise Strategy, Establishing a Cloud-Incorporated Business Strategy

UNIT-V

Transitioning to Cloud-Centric Enterprises The Tuning Methodology, Contract Management in the Cloud Cloud-Instigated IT Transformations Introduction, Explaining Cloud Infrastructures, A Briefing on Next-Generation Services, Service Infrastructures, Cloud Infrastructures, Cloud Infrastructure Solutions, Clouds for Business Continuity, The Relevance of Private Clouds, The Emergence of Enterprise Clouds

TEXT BOOKS:

1. Erl Thomas, Puttini Ricardo, Mahmood Zaigham, Cloud Computing: Concepts, Technology & Architecture 1st Edition,

2. Pethuru Raj, Cloud Enterprise Architecture, CRC Press

REFERENCE:

1. James Bond, The Enterprise Cloud, O'Reilly Media, Inc.

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-III Semester-VLSI Design

Course Code: 25BVL27

DISSERTATION PHASE-I

L	T	P	C
0	0	20	10

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-III Semester-VLSI Design

Course Code: 25BVL28

INDUSTRY INTERNSHIP

L	T	P	C
0	0	0	2

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-III Semester-VLSI Design

Course Code: 25BVL29

CO-CURRICULAR ACTIVITIES

L	T	P	C
0	0	0	1

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

M.Tech-IV Semester-VLSI Design

Course Code: 25BVL30

DISSERTATION PHASE-II

L	T	P	C
0	0	32	16